Dallas Semiconductor

Product Data Book 1987

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DALLAS SEMICONDUCTOR CORPORATION
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Dallas Semiconductor
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Dallas Semiconductor
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Corporate Fact Sheet

Dallas Semiconductor designs, manufactures and markets CMOS integrated circuits using special Late Definition technology. Late Definition permits the exact definition of a product to be postponed until end use, thereby increasing flexibility.

PRODUCTS

Founded February 1, 1984, Dallas Semiconductor has a multi-products strategy to serve the needs of the computer and communications industry. Our optimism stems from the ability to sell "soft silicon" which can be readily tailored to solve the specific problems of our customers. Soft silicon results from the Late Definition technologies of lithium, laser, and implant. Lithium postpones definition until end use, thereby making the chip adaptive in the system. Laser pospones definition until just before the chip is placed in the package, and implant postpones definition until the last wafer process step.

LITHIUM

Advances in CMOS circuitry have reduced power requirements to the point that a chip, using appropriate circuitry, can be packaged with a miniature lithium energy source which will last the useful life of the equipment. This allows Dallas Semiconductor to make chips which don't forget. Our initial product offerings exploited this capability to make the much sought-after nonvolatile RAM. In November 1984 we began shipping 16K, 64K RAMs.

Keeping track of human time has not been an easy task for computers until our July 1985 announcement of the DS1216 SmartWatch. It precisely keeps calendar time down to the hundredth of a second, replacing what heretofore consumed a whole printed circuit board full of electronics. A lithium cell provides power for life. Under development are products which take full advantage of the adaptive nature of lithium-based products, meaning that they can capture data in real time, remember it indefinitely, and use the information to improve system performance.

LASER

The laser creates uniqueness on a chip at low cost. The sub-micron positioning laser and formidable control software developed at Dallas can engrave individual chips with digital patterns making each one different. These after-the-fact changes to completed circuits give our laser-based products a competitive edge.

The first product that demonstrates our special laser technology is an extremely accurate time base, commonly referred to as a delay line. Before the August 1985 announcement date, it had only been possible to build such devices using a dozen components in a hybrid assembly. The DS1000 Silicon Delay Line series is a direct replacement for hybrid delay lines which are widely used in conjunction with DRAMs and Winchester disks.

Other products use the laser to protect sensitive information and intellectual property by creating a powerful security mechanism in micro chips. The DS1204 Electronic Key is an example of a product which benefits from the laser in this regard. Exclusive blank Keys are defined by laser for each customer, adding to the overall security mechanism. Additional products are on the drawing board whereby the laser tailors the option content of the chip for a particular customer. In short, the laser lets Dallas Semiconductor define each chip uniquely after it is already operational.

IMPLANT

High energy ion implant technology will be put into operation in 1987. Nearly-finished wafers can be defined to meet exact customer requirements in a matter of days. A number of products will be offered with an "Express Delivery Service."

Difficult system problems have been solved by relying on these special technologies, experience, and creativity, to offer our customers a more complete solution than the chip alone can provide. Often this requires a greater emphasis on packaging than traditional semiconductor producers have been accustomed. Twenty-seven products were

put into production prior to July 1986, unified by Late Definition technology.

MARKETING AND SALES
Dallas Semiconductor sells to OEMs through domestic sales offices, a network of manufacturers' representatives and distributors worldwide.

MANUFACTURING AND FACILITIES
Dallas Semiconductor manufactures products at a 65,000-square-foot facility, which it owns, located at the company's headquarters in north Dallas. All product is shipped from Dallas after final quality assurance testing.

CORPORATE DATA
Dallas Semiconductor raised more than $36M in venture capital and bond financing, making it one of the industry's best-financed high technology start-ups. A private placement of stock from the group of venture capital investors includes Southwest Enterprise Associates, New Enterprise Associates, Ventech Partners, Oak Investment Partners, Merrill Pickard Anderson & Eyre, John Hancock Venture Capital Fund, Merrill Lynch Venture Partners, Arscott Norton & Associates, Venture Growth Associates, Crossroads Capital, Abingworth, J.F. Shea, First Source, New Venture, and Republic Bank. The company has assembled a superb technical team of engineering professionals. Vin Prothro, a former president of Mostek, is Chairman of the Board.

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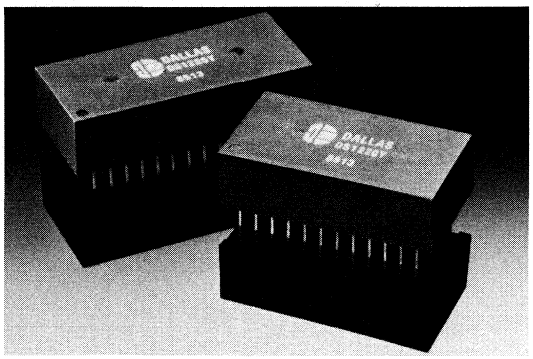
Product Overview

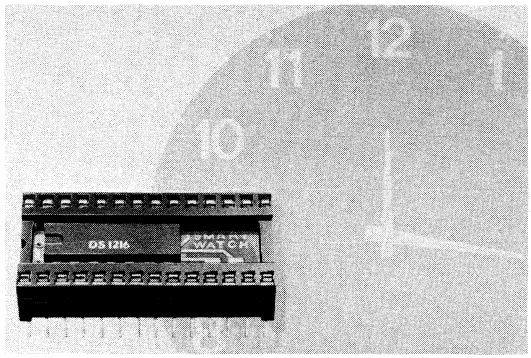
NONVOLATILE SRAMS



Nonvolatile RAM stores 64K

The **DS1225** is an 8K × 8 nonvolatile CMOS static RAM that reads or writes in 150 nanoseconds. Designed to supercede a variety of EEPROMs, the RAM has unlimited write cycle endurance. The 28-pin memory has a self-contained lithium energy source to retain data for more than 10 years in the absence of power. Automatic write protection prevents data from being garbled during power fluctuations. The **DS1220** is a 24-pin 2K × 8 version.

INTELLIGENT SOCKETS



SmartSocket, SmartWatch

When the **DS1213** SmartSocket is mated with a CMOS RAM, either 28-pin 8K × 8 or 24-pin 2K × 8 lower-justified, it makes the RAM contents nonvolatile by automatically switching to an internal lithium source and write protecting on the occurrence of power interruption. **DS1213C** accepts 8K × 8 or 32K × RAMs.

SmartWatch DS1216 has all the features of the SmartSocket plus the ability to stamp and date events. A built-in CMOS chip makes available time from a hundredth of a second to minutes, hours, days and years. If external power fluctuates or goes away, the device is automatically energized by an internal lithium source for more than 10 years. Access to time-of-day information occurs without disturbing mated memory. The timekeeping function has a phantom interface that is activated on software demand only when needed. **DS1216E** accepts ROMs or EPROMs.

USER INSERTABLE MEMORY

DS1217 Cartridge

In addition to being nonvolatile read/write, this up to 1 M bit memory cartridge can be inserted by the end user. A simple ribbon cable adaptor **DS9000** connects it to an existing 28-pin JEDEC Byte Wide socket. The cartridge is a 250 ns replacement for bubble memory and retains data for more than 10 years. Densities from 2K × 8 to 128K × 8 are available.

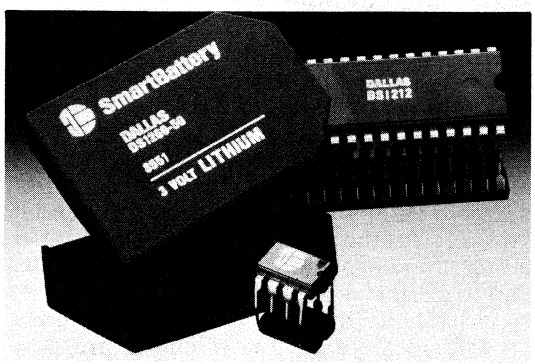
Electronic Tag

This miniature nonvolatile RAM is durable enough to withstand vigorous use. Carried in a shirt pocket, stored in a desk drawer or even dropped in water, the user insertable tag retains memory for more than a decade. The **DS1201** easily connects to any system via a five-pin SIP strip and access data in 250 ns.

KeyRing

The **DS1250** KeyRing connects Electronic Tags DS1201 or Keys DS1204 to any system which uses Byte Wide semiconductor memory. The socket end of the KeyRing fits on the system's RAM, ROM, or EEPROM, and is connected to a 5-position clip via a thin cable. The clip's adhesive backing permits easy attachment to a system enclosure. The KeyRing contains a CMOS integrated circuit which redirects information flow from the system memory to the inserted Tag. Once installed, communication to the Tag is totally controlled by software.

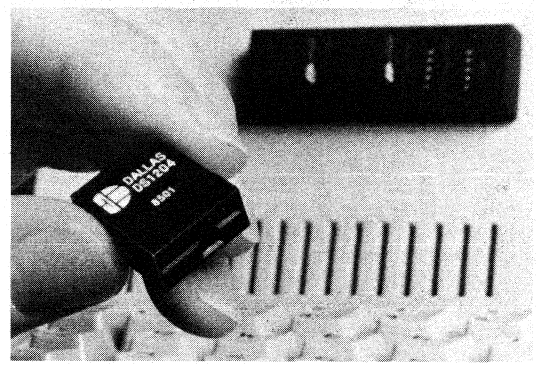
INTEGRATED BATTERY BACKUP



Three-Part CMOS Chip Set "Crash-Proofs" Processor-Based Systems

Integrated Battery Back-Up is a three-part CMOS chip set which allows the orderly shutdown and automatic restart of microprocessor-based systems. The **DS1231** Power Monitor warns the processor of power failure so that critical data can be stored before power loss; the **DS1212** Nonvolatile Controller/Decoder safeguards up to 16 CMOS RAMs of data during power transients; and the **DS1260** SmartBattery sources 1 A-hr of lithium energy, providing uninterruptable power to maintain data. The **DS1221** Nonvolatile Controller/Decoder safeguards four RAMs, the **DS1210** a single RAM.

SOFTWARE AUTHORIZATION



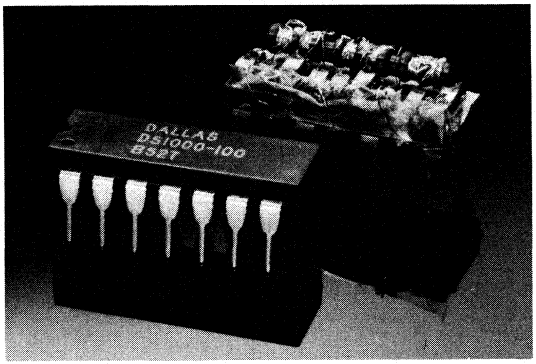
Electronic Key

DS1204 Electronic Key is a postage-stamp-sized semiconductor that is changing the shape of software copy protection. Semiconductor-based hardware "keys" allow individual users unlimited private use and backups of software while protecting software makers against piracy. Sofware publishers then program the keys and include them with each package they sell. Backup copies can be made but the key must be present whenever users want to run the software.

Software Authorization Kit

The **DS1253K** Software Authorization Kit includes: **DS1204S** Electronic Key, **DS1201S** Electronic Tag, **DS1253** KeyRing, Demonstration software for IBM PC on floppy disk, documentation, source listing and data sheets. The **DS1253** KeyRing connects up to 5 Electronic Keys DS1204S, Tags DS1201S, and TimeKeys DS1207 to the IBM PC Parallel Printer Port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the printer port adapter, and reconnecting the printer to back connector on the printer port adapter.

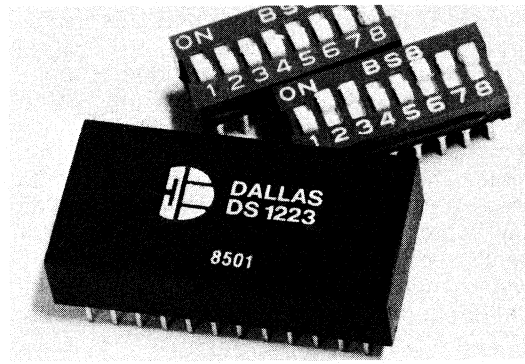
SILICON TIMED CIRCUITS



Silicon Time Delays

New all-silicon CMOS time delay devices (left) from Dallas Semiconductor offer single-chip reliability and significantly greater economy than conventional hybrid delay lines (right, with cover removed) due to their laser-defined specifications. TTL-compatible, the **DS1000** Series Delay Lines have five equally-spaced taps, providing delays from 20 ns to 500 ns. They represent the first major technological advance for delay products in nearly 20 years, and can serve as drop-in replacements for the delay lines made under the older hybrid methods. Using less than half the power of conventional delay lines, the DS1000 is available as a standard low-profile, 14-pin DIP that permits automatic insertion; or in an 8-pin surface-mountable package. The **DS1030** DRAM Timer series is the most economical way of generating the precise time delays for dynamic RAM applications. Silicon Delay Lines are available as catalog items from stock, as well as made-to-order time delays.

SYSTEM EXTENSION



Electronic Configurator

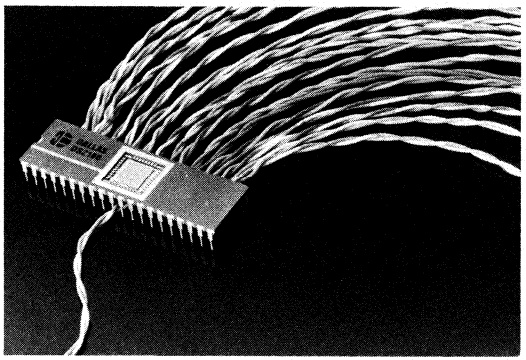
The **DS1223** Electronic Configurator is a CMOS circuit, backed by an embedded lithium energy source which can be programmed remotely to configure as many as 16 signal lines. The settings can be retained for at least a decade without any system power. Menu-driven software can be used to control switch settings through an on-chip serial port. Each of the switching pins can be set in a high (5V) or low (ground) state as well as tied to an adjacent pin through a serial port. Nine additional bytes of NV RAM are included on chip to store printed circuit board part number, revision status, serial number, and service history.

Phantom Interface

The **DS1206** Add-On Serial Port provides a minimum cost interface to the DS1201 Electronic Tag, the DS1204 Electronic Key, and the DS1223 Configurator by intercepting the standardized memory bus found in computer systems. A three wire serial port is derived from the memory address bus without affecting address space, thereby maintaining transparency to the memory bus. Communication is established under software control by an address pattern recognition sequence which disables an individual Byte Wide/ DRAM memory via CE/CAS signals. Upon completion the serial transfer, the disabled system memory is automatically reconnected to the memory bus.

DS1222 BankSwitch
The DS1222 BankSwitch is a software controlled one-of-sixteen selector. Highly structured address sequences are recognized and used to set each of the sixteen states. Applications include expansion of processor memory address range and software controlled write protection for nonvolatile read/write memories.

T1 TELECOMMUNICATIONS



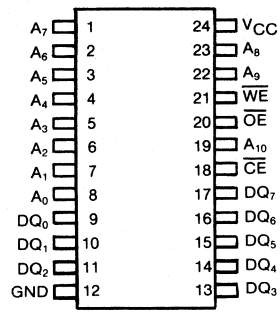
DS2180 Single Chip Transceiver Links to Bell System T1 Digital Lines
T1, developed by AT&T in the early 60s, can carry digitized voice and/or data services at 1.5 million bits per second, 150 times faster than modem-based information networks. The transceiver, a 40-pin CMOS VLSI device, is compatible with existing and emerging network transmission standards allowing interconnect to the more than 100 million circuit miles of installed T-carrier. The **DS2176** T1 Receive Buffer synchronizes incoming data to system clock. The **DS2185** Line Interface eliminates analog components previously required to connect to twisted-pair transmission line.

Dallas Semiconductor
16K Nonvolatile Memory Module — *DS1220*

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- 200 ns read access time
- Read cycle time equals write cycle time
- Full ± 10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated DS1220IND

PIN CONNECTIONS



PIN NAMES

A_0-A_{10}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable

DESCRIPTION

The DS 1220 is a 16,384 bit fully static nonvolatile memory module organized as 2048 words by 8 bits. The nonvolatile memory module has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out of tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile memory module can be used in place of existing 2K x 8 static RAM directly conforming to the popular byte wide 24 pin DIP standard. The DS1220 also matches the pinout of the 2716 EPROM or the 2816 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220 is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile RAM module provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 V nominal. Data is maintained in the absence of V_{CC} without additional support circuitry. The DS1220 constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		$V_{CCI}+0.3$	V	
Input Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	*u*A	
I/O Leakage Current	I_{LO}	−5.0		+5.0	*u*A	
Output Current @ 2.4V	I_{OH}	−1.0	−2.0		mA	
Output Current @ 0.4V	I_{OL}	2.0	2.0		mA	
Standby Current CE = 2.2V	I_{DDS1}		3.0	7.0	mA	
Standby Current CE $V_{CC}-0.5V$	I_{DDS2}			4.0	mA	
Operating Current	I_{DDO1}			75	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

($t_A = 25°C$)

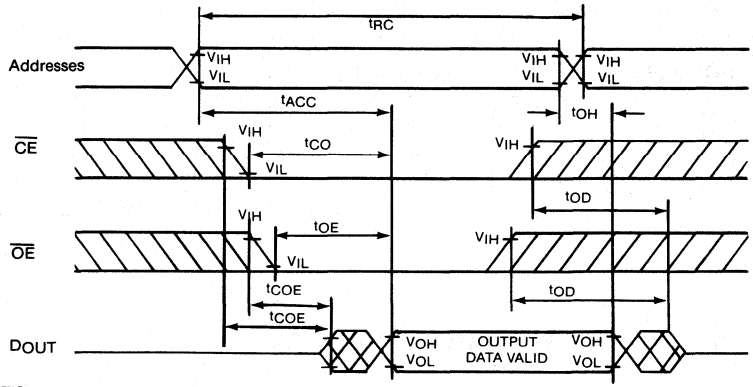
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

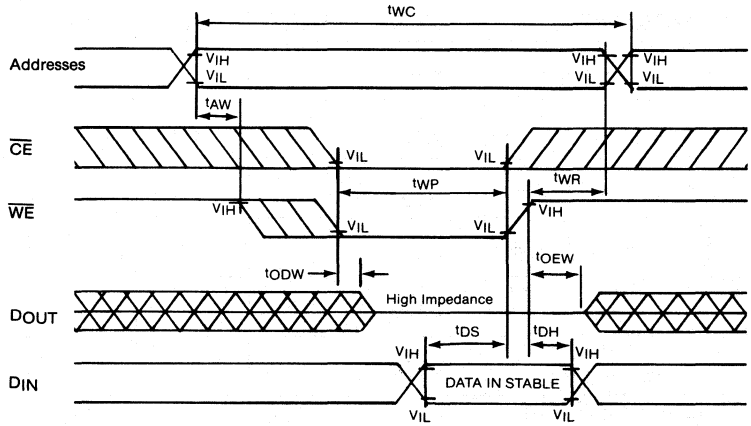
(0°C to 70°C, V_{CC} = 5.0V ± 10%)

		DS1220-150		DS1220-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{OE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10		10		ns	
Output High Z from Deselection	t_{OD}		70		100	ns	
Output Hold From Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		170		ns	3
Address Set Up Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		70		80	ns	
Output Active From $\overline{WE}$	t_{OEW}	10		10		ns	
Data Setup Time	t_{DS}	60		90		ns	4
Data Hold Time	t_{DH}	0		0		ns	4,5

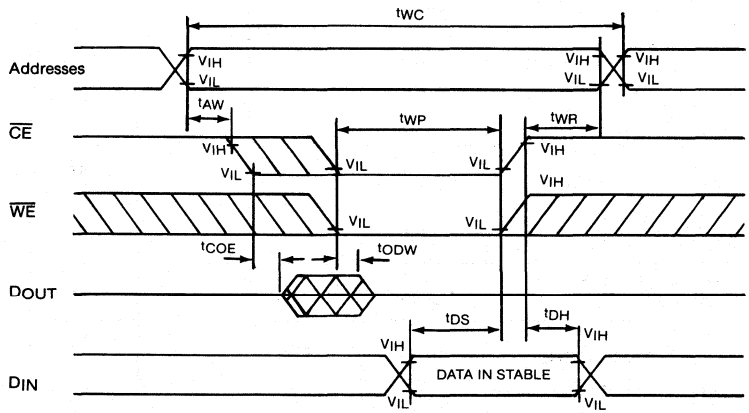
READ CYCLE (1)



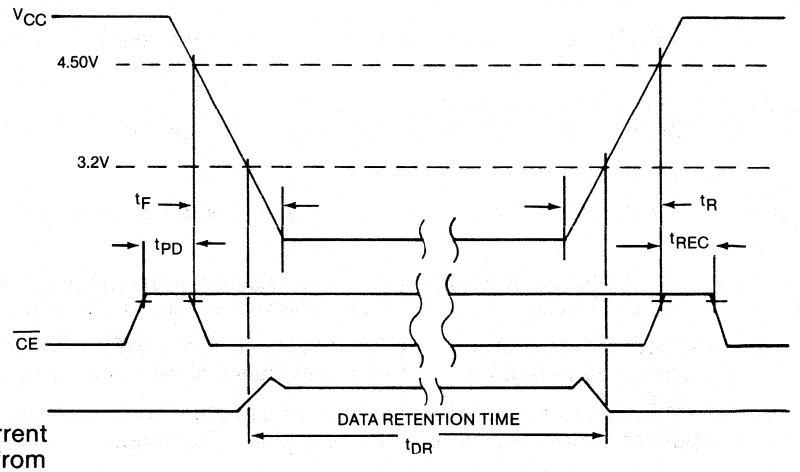
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		µs	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up		2	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then t_{DH} = 20ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1220 is market with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

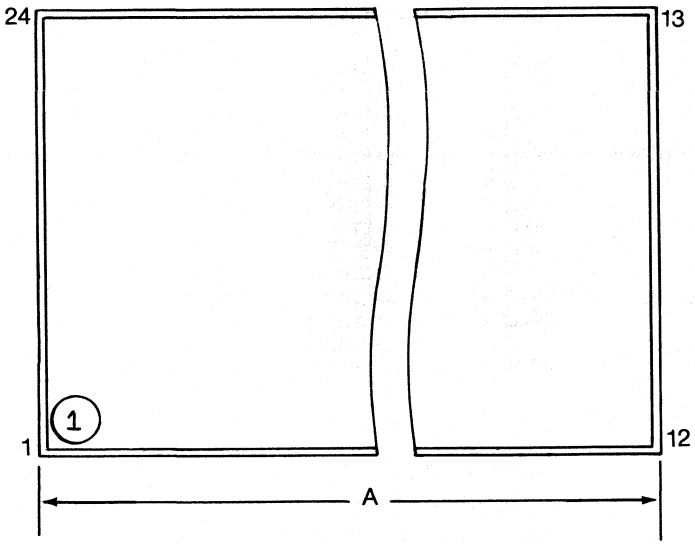
D.C. Test Conditions

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

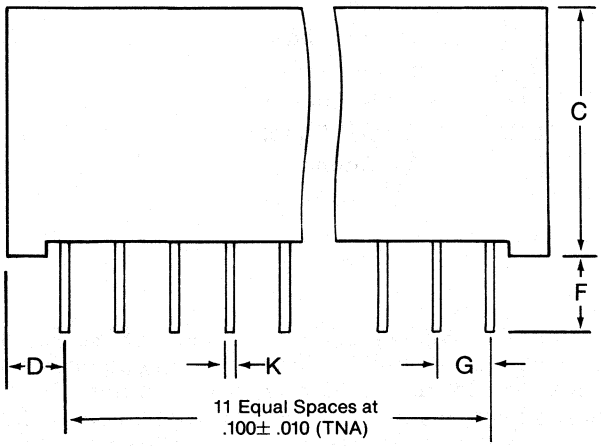
A.C. Test Conditions

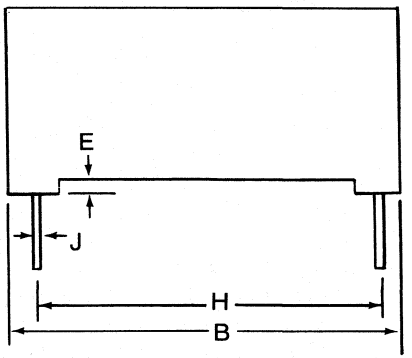
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS1220Y
Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.320	1.340
B	.695	.720
C	.395	.410
D	.090	.130
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021

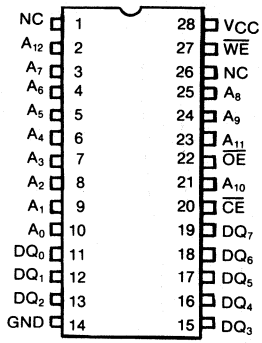




Dallas Semiconductor
64K Nonvolatile Memory Module — DS1225

FEATURES
- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28 pin JEDEC pinout
- Available in either 150 or 200 ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated DS1225IND

PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

DESCRIPTION
The DS1225 is a 65,536-bit, fully static, nonvolatile memory module organized as 8192 words by 8 bits. The nonvolatile memory module has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile memory module can be used in place of existing 8K × 8 static RAM directly conforming to the popular byte wide 28 pin DIP standard. The DS1225 also matches the pinout of the 2764 EPROM or the 2864 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225 is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile RAM module provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1225 constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	-0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	μA	
I/O Leakage Current	I_{LO}	-1.0		+1.0	μA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE} > V_{CC}$ -0.5V	I_{CCS2}			4.0	mA	
Operating Current	I_{CC01}			50	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

($t_A = 25°C$)

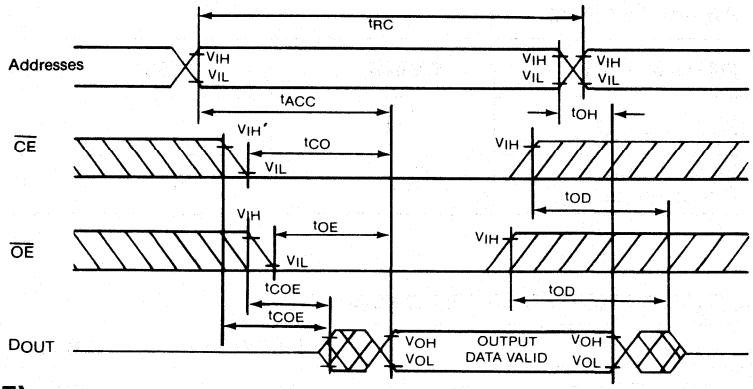
PARAMETER	SYMBOL	TYP.	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

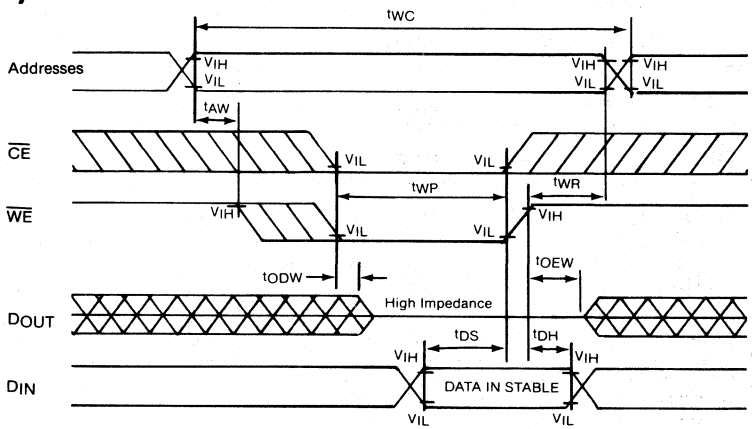
(0°C to 70°C, V_{CC} = 5.0V ± 10%)

		DS1225-150		DS1225-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{OE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10		10		ns	
Output High Z from Deselection	t_{OD}		70		100	ns	
Output Hold From Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		170		ns	3
Address Set Up Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		70		80	ns	
Output Active From $\overline{WE}$	t_{OEW}	10		10		ns	
Data Setup Time	t_{DS}	60		90		ns	4
Data Hold Time	t_{DH}	0		0		ns	4,5

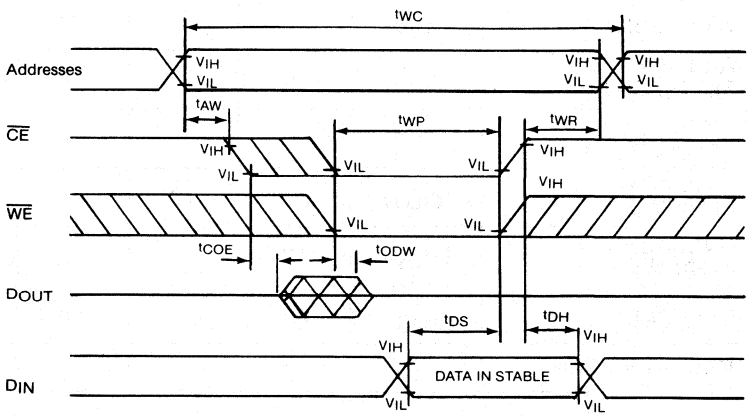
READ CYCLE (1)



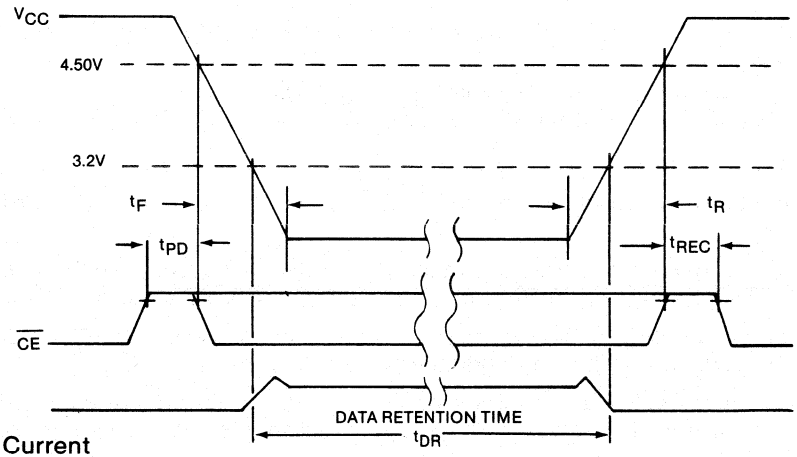
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L Supplied from
Lithium Cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up		2	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ low transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1225 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

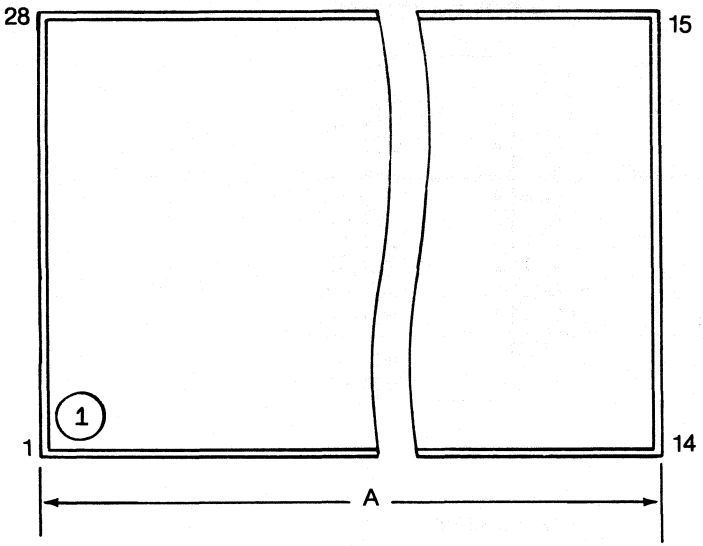
D.C. Test Conditions

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

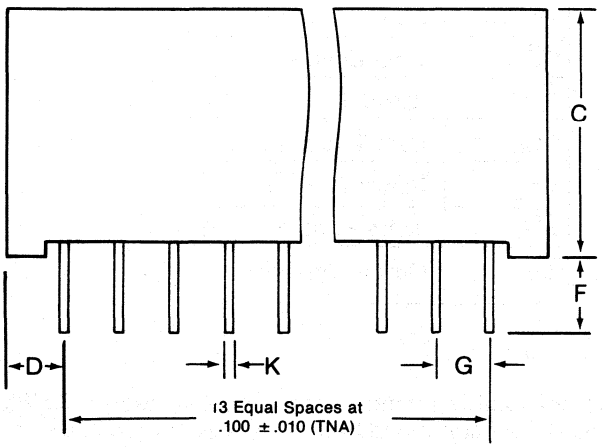
A.C. Test Conditions

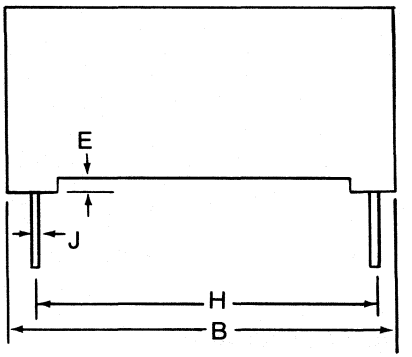
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

DS1225Y
64K Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.520	1.540
B	.695	.720
C	.395	.410
D	.090	.120
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





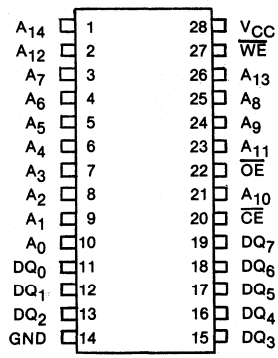
Dallas Semiconductor
256K Nonvolatile RAM

DS1230

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28 pin JEDEC pinout
- 150ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range

PIN CONNECTIONS



PIN NAMES

A_0-A_{14}	Address Inputs
$\overline{CE}$	Chip Enable
GND	Ground
DQ_0-DQ_7	Data In/Data Out
V_{CC}	Power (+5 V)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

DESCRIPTION

The DS1230 is a 262, 144 bit fully static nonvolatile memory module organized as 32768 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out of tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile memory module can be used in place of 32K × 8 static RAM directly conforming to the popular byte wide 28 pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

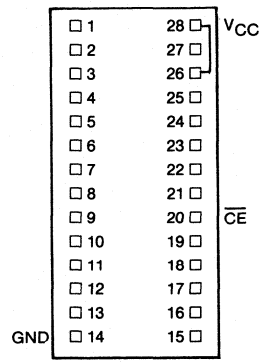
Dallas Semiconductor

SmartSocket — *DS1213*

FEATURES

- Accepts standard 2K × 8 and 8K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K × 8 to 8K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN CONNECTIONS



PIN NAMES

All pins pass through except 20, 26, 28.

Pin 20 $\overline{CE}$ - Conditioned Chip Enable
Pin 26 V_{CC} - Switched V_{CC} for 24-pin RAM
Pin 28 V_{CC} - Switched V_{CC} for 28-pin RAM
Pin 14 GND - Ground

DESCRIPTION

The DS1213 is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 28-pin 8K × 8 or 24-pin 2K × 8 lower-justified JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28, 26, 20 and 14 for RAM control. All other pins are passed straight through to the socket receptacle.

OPERATION

The DS1213 SmartSocket performs five circuit functions required to battery back-up a CMOS memory. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartSocket provides is power fail detection. Power fail detection occurs between 4.75 and 4.5 volts. The DS1213 constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of VCC or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213 performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function which the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to insure reliability. The DS1213 SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cells contains 35 mA/hr capacity, making the total 70 mA/hr.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1,3
Logic 1 PIN 20 L	V_{IH}	2.2		V_{CC}+0.3	V	1,3
Logic 0 PIN 20 L	V_{IL}	-0.3		+0.8	V	1,3

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
PIN 26 U, PIN 28 U Supply Voltage	V_{CCO}	V_{CC} -0.2			V	3, 8
PIN 26 U, PIN 28 U Supply Current	I_{CCO}			80	mA	3, 8
PIN 20 L $\overline{CE}$ Input Leakage	I_{IL}	-1.0		+1.0	μA	3, 4
PIN 20 U $\overline{CE}$ Output @ 2.4V	I_{OH}	-1.0			mA	2, 3
PIN 20 U $\overline{CE}$ Output @ .4V	I_{OL}			4.0	mA	2, 3

(0°C to 70°C, V_{CC} < 4.5V)

PIN 20 U Output	V_{OHL}	V_{CC} -0.2 V_{BAT} -0.2			V	3
PIN 26 U, PIN 28 U Battery Current	I_{BAT}			1	μA	3, 6
PIN 26 U, PIN 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE

($t_A = 25\,°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance PIN 20 L	C_{IN}	5	pF	3
Output Capacitance PIN 20 U	C_{OUT}	7	pF	3

A.C. ELECTRICAL CHARACTERISTICS

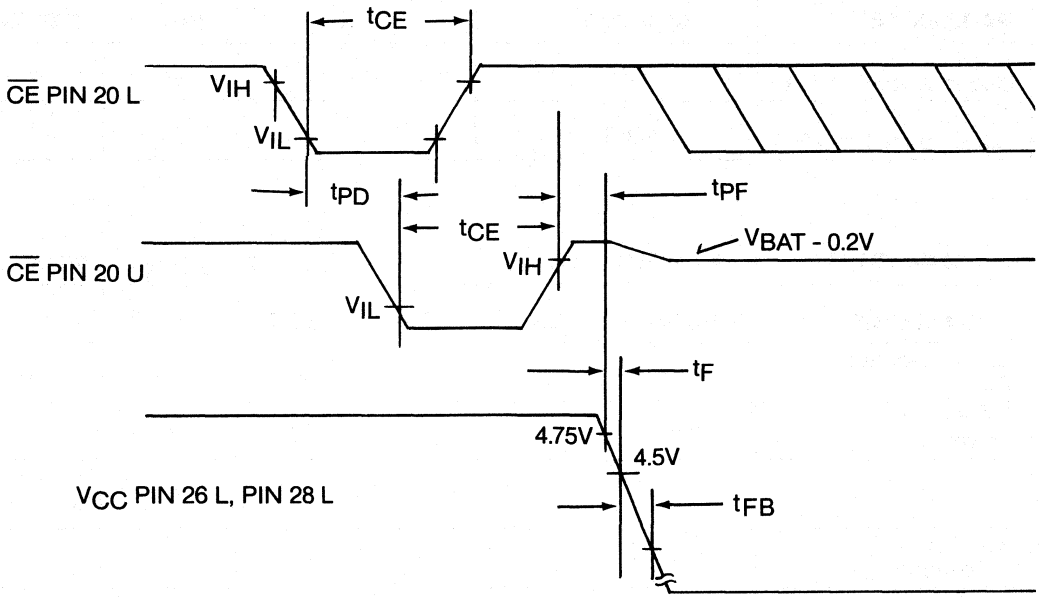
(0 °C to 70 °C, $V_{CC} = 4.75$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

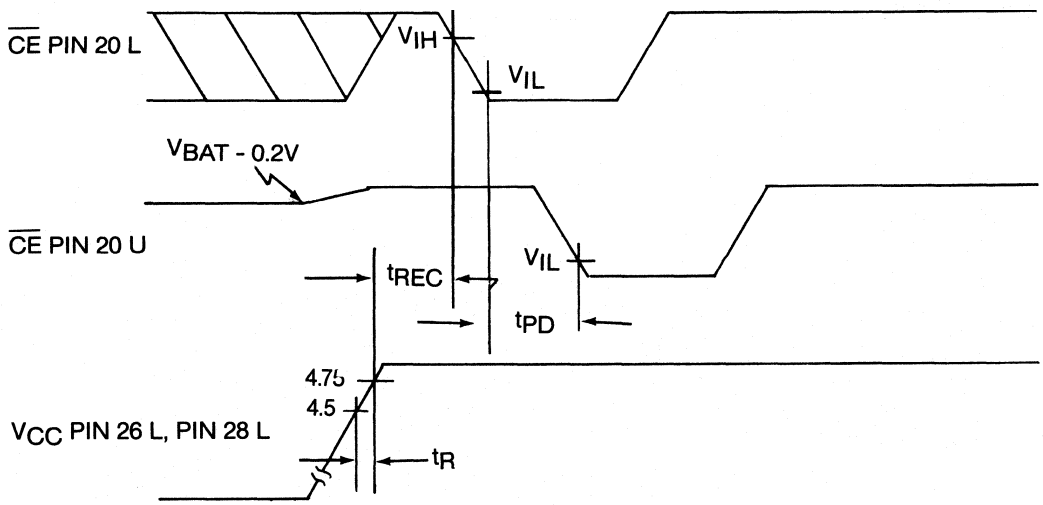
(0 °C to 70 °C, $V_{CC} < 4.5V$)

Recovery at Power up	t_{REC}		80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5 V	t_F	300			μs	
V_{CC} Slew Rate 4.5 - 3 V	t_{FB}	10			μs	
V_{CC} Slew Rate 4.5 - 4.75 V	t_R	0			μs	

TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP

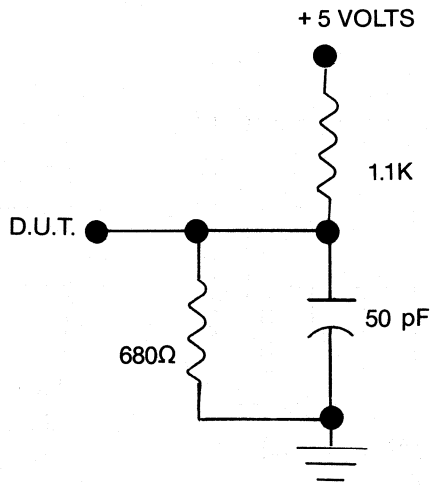


NOTES:

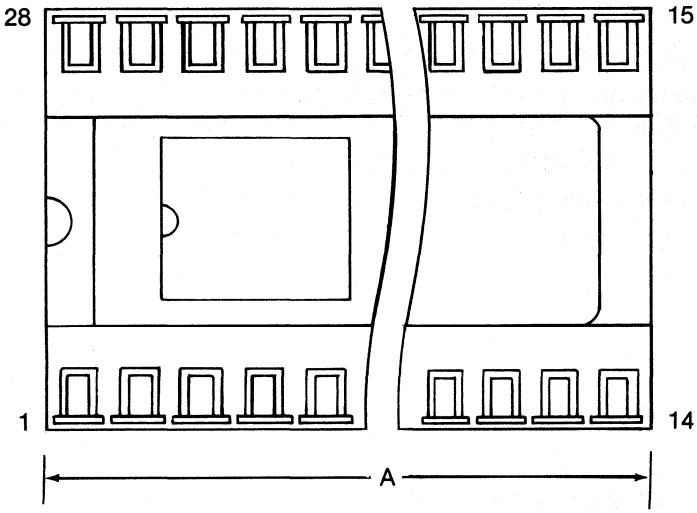
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26 L may be connected to V_{CC} or left disconnected at the P.C. board.
6. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to insure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD

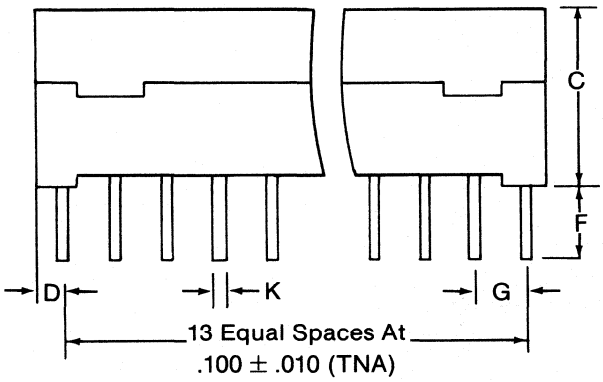
Figure 1

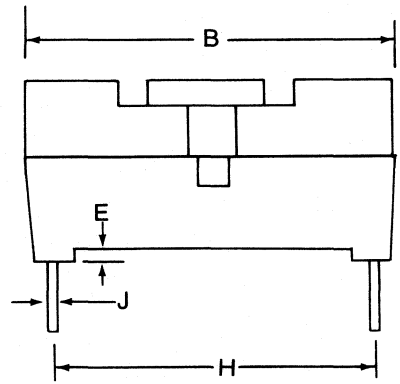


DS1213
SmartSocket



DIM.	INCHES	
	MIN.	MAX.
A	1.390	1.420
B	.695	.710
C	.350	.370
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





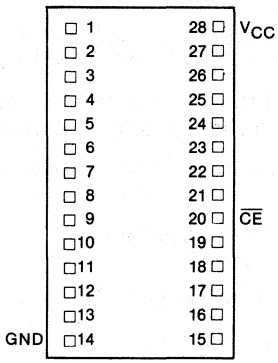
Dallas Semiconductor
SmartSocket

DS1213C

FEATURES

- Accepts standard 8K × 8 and 32K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K × 8 to 32K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN CONNECTIONS



PIN DEFINITIONS

All pins pass through except 20, 28.

Pin 20 conditioned Chip Enable
Pin 28 switched V_{CC}
Pin 14 ground

DESCRIPTION

The DS1213C is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K × 8 or a 32K × 8 JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

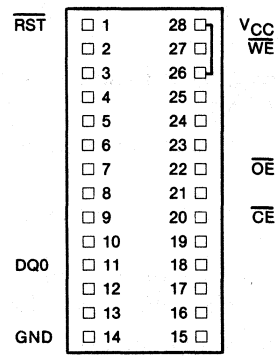
Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28 and 20 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213 data sheet for technical details.

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K × 8 and 8 K×8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

PIN CONNECTIONS



PIN DEFINITIONS

All Pins Pass Through Except
20, 26, 28
Pin 20 Conditioned Chip Enable
Pin 26 Switched V_{CC} for 24 Pin RAM
Pin 28 Switched V_{CC} for 28 Pin RAM
Pin 1 $\overline{RESET}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

DESCRIPTION

The DS1216 is a 28-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K × 8 or 28-pin 8K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors V_{CC} for an out of tolerance condition. When such a condition occurs, an internal

lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

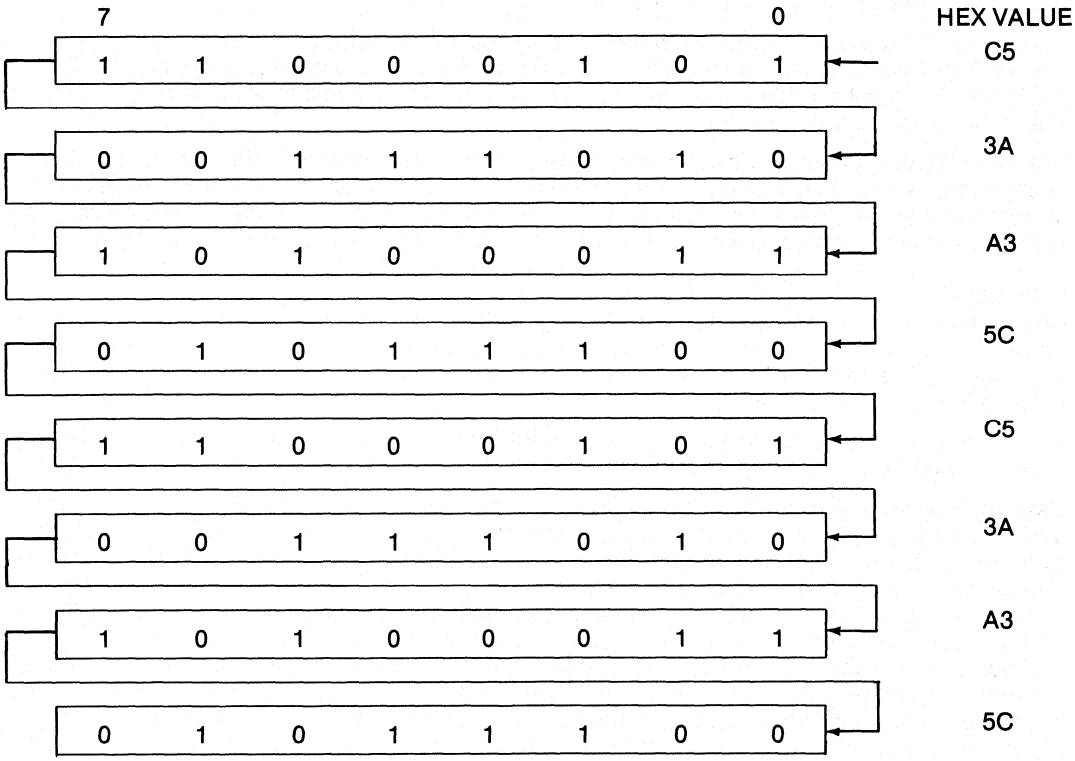
OPERATION

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64 bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CE}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch, therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure1



NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}.

NONVOLATILE CONTROLLER OPERATION
The DS1216 SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which is involved provides is power fail detection. Power fail detection occurs at typically 4.25 volts. The DS1216 constantly monitors the V_{CC} supply. When V_{CC} goes out of tolerance, a comparator outputs a power fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of V_{CC} or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64 bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12 hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24 hour mode, bit 5 is the second 10-hour bit (20-23 hours).

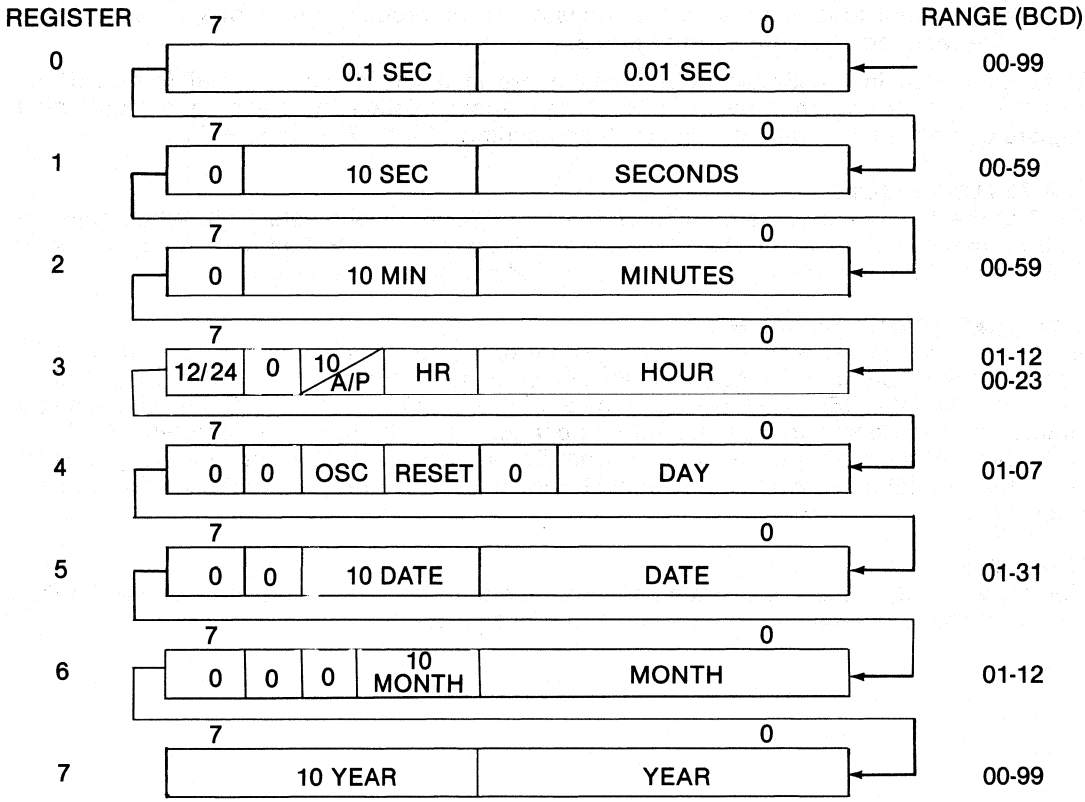
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −1.0V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1, 10
Logic 0	V_{IL}	−0.3		+0.8	V	1, 10

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PIN 26L, PIN 28L Supply	I_{CCI}			5	mA	3, 4, 5
PIN 26U, PIN 28U Supply Voltage	V_{CCO}	$V_{CC}-0.2$			V	3, 8
PIN 26U, PIN 28U Supply Current	I_{CCO}			80	mA	3, 8
Input Leakage	I_{IL}	−1.0		+1.0	μA	4,10, 13
Output @ 2.4V	I_{OH}	−1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°, V_{CC} < 4.5V)

PIN 20U Output	V_{OHL}	$V_{CC}-0.2$ $V_{BAT}-0.2$			V	3
PIN 26U, PIN 28U Battery Current	I_{BAT}			1	μA	3, 6
Pin 26U, PIN 28U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

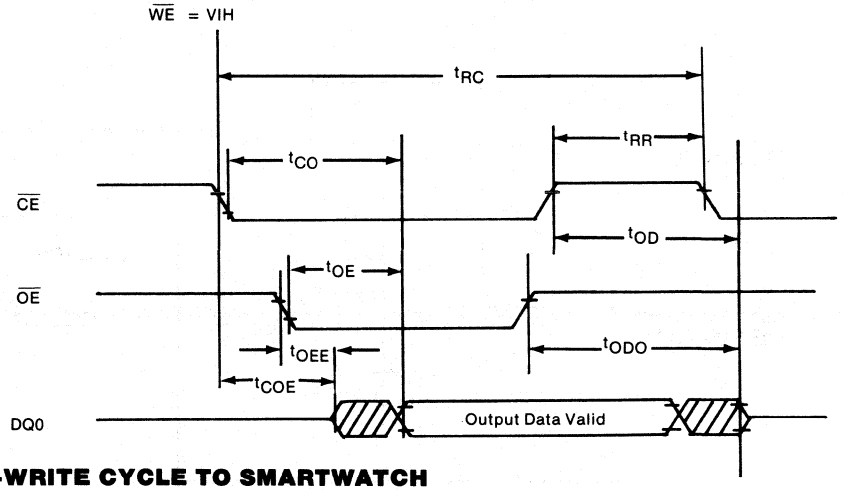
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	11
Data Set Up Time	t_{DS}	100			ns	11
Data Hold Time	t_{DH}	0			ns	12
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
Reset Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

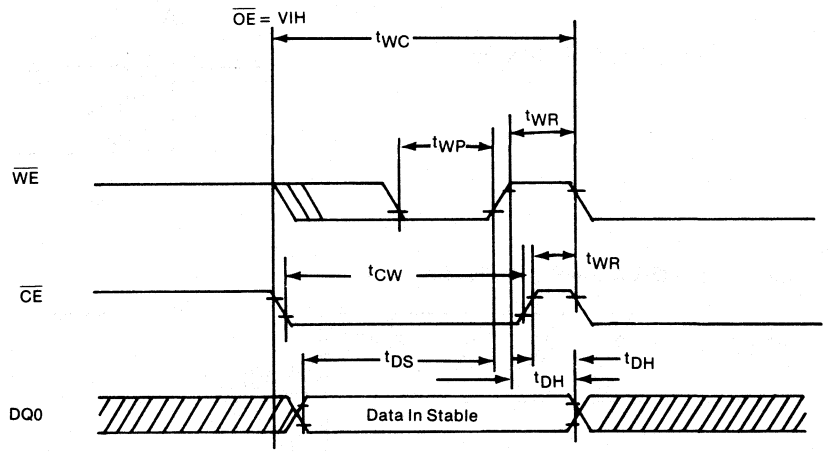
(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}	2	5	10	ms	
V_{CC} Slew Rate 4.5 - 3V	t_F	300			μs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	μs	7

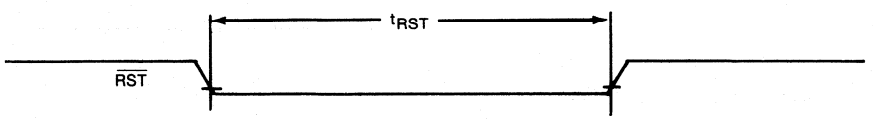
TIMING DIAGRAM—READ CYCLE TO SMARTWATCH



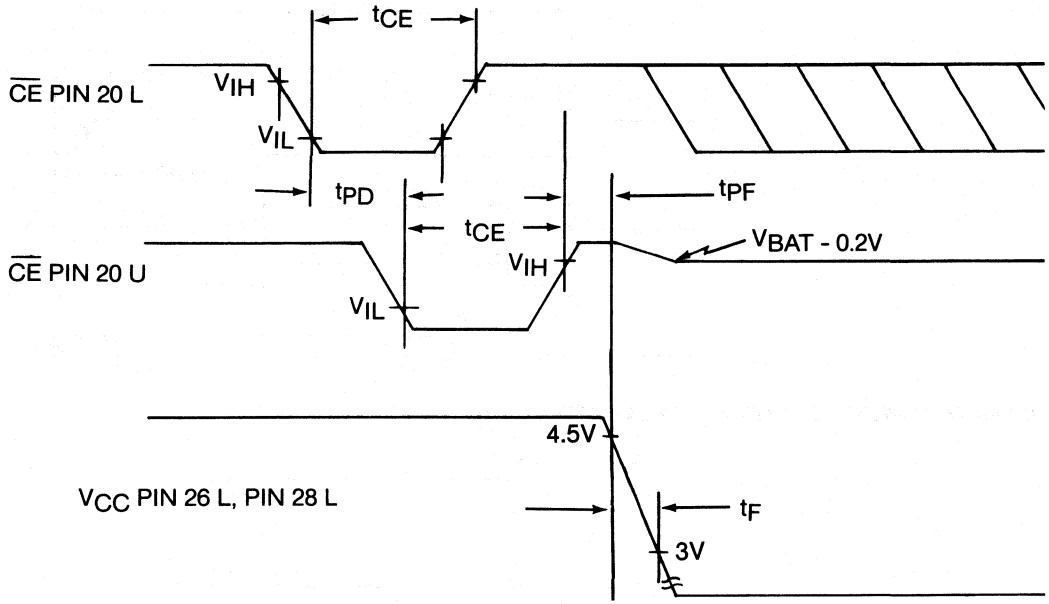
TIMING DIAGRAM—WRITE CYCLE TO SMARTWATCH



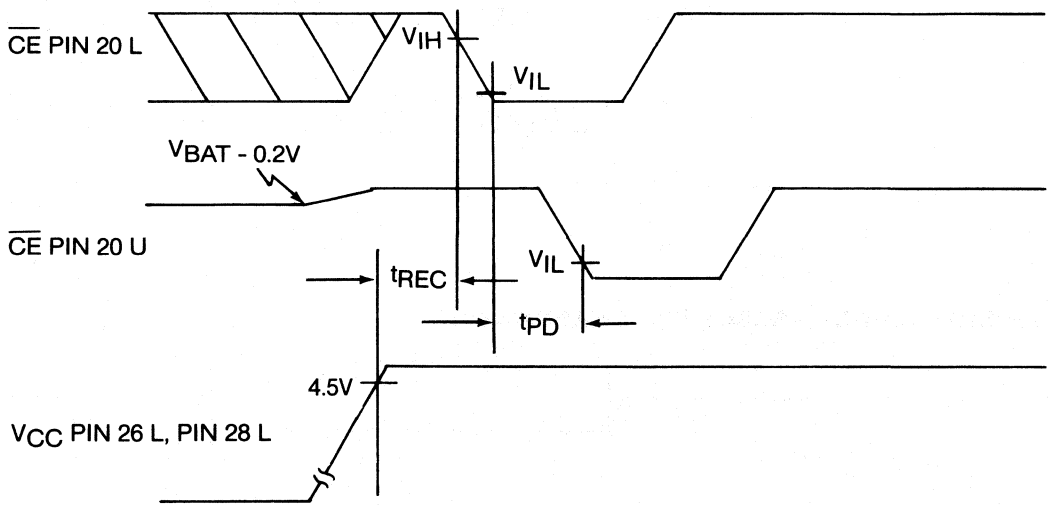
TIMING DIAGRAM—RESET FOR SMARTWATCH



TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP

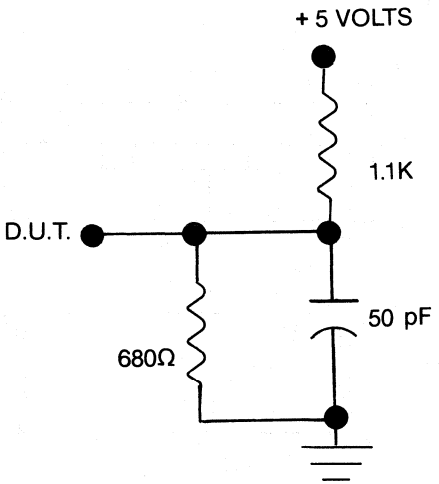


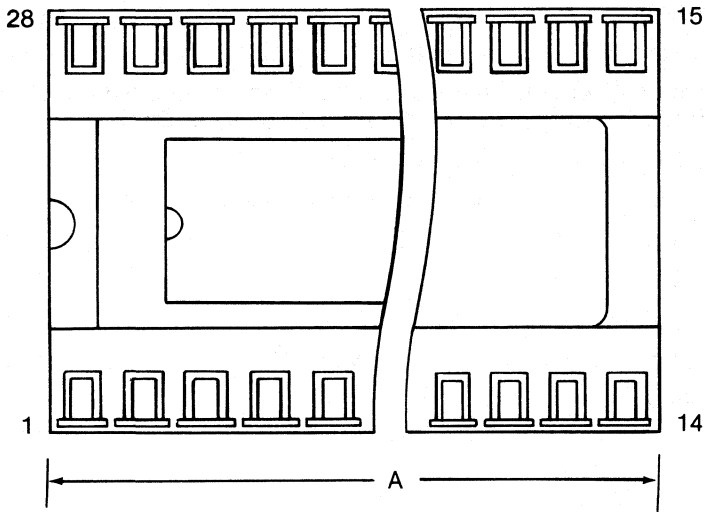
NOTES

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. PIN locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. PIN 26 L may be connected to V_{CC} or left disconnected at the P.C. board.
6. I_{BAT} is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25 °C.
7. t_{CE} max. must be met to insure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L
11. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$
12. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$
13. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

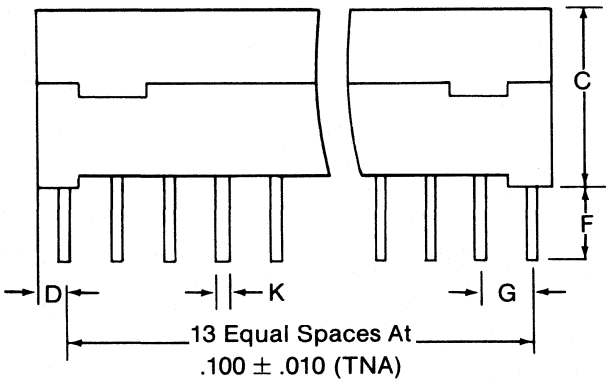
OUTPUT LOAD

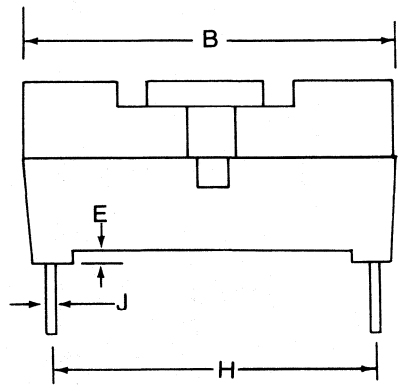
Figure 3





DIM.	INCHES	
	MIN.	MAX.
A	1.390	1.420
B	.695	.710
C	.350	.370
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021

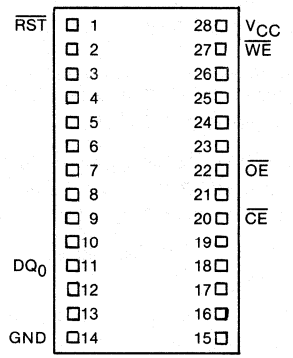




FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K × 8 and 32K × 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

PIN CONNECTIONS



PIN DEFINITIONS

All Pins Pass Through Except 20, 28
Pin 20 Conditioned Chip Enable
Pin 28 Switched V_{CC}
Pin 1 $\overline{RESET}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

DESCRIPTION

The DS1216C is a 28-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K × 8 or a 32K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216 data sheet for technical details.

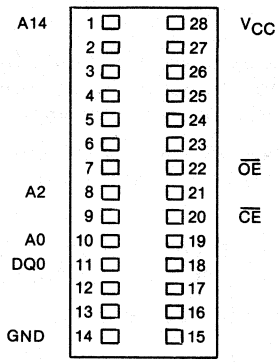
Dallas Semiconductor
SmartWatch

PRELIMINARY
DS1216E

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC Byte Wide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accurate to within 1 min./month @25°C

PIN CONNECTIONS



PIN NAMES

Pin 1 A14 - Address Bit 14 ($\overline{RESET}$)
Pin 8 A2 - Address Bit 2 (READ/$\overline{WRITE}$)
Pin 10 A0 - Address Bit 0 (Data Input)
Pin 11 DQ0 - I/O_0 (Data Output)
Pin 14 GND - Ground
Pin 20 $\overline{CE}$ - Conditioned Chip Enable
Pin 22 $\overline{OE}$ - Output Enable
Pin 28 V_{CC} - +5 VDC to the Socket

All pins pass through to the Socket except 20.

DESCRIPTION

The DS1216E is a 28-pin, 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device take up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20 and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 ($\overline{CE}$) which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnect the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals $\overline{OE}$ and $\overline{CE}$, and Data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit A0. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal ($\overline{OE}$ or $\overline{CE}$) must transition low to begin and high to end memory cycles which are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle. Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch insuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of READ/$\overline{WRITE}$ (A2). Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ and $\overline{OE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 ($\overline{RESET}$) low, if enabled, or on power up. This $\overline{RESET}$ can occur during pattern recognition or while accessing the SmartWatch registers. $\overline{RESET}$ causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. The second function provides power fail detection. Power fail detection occurs at typically 4.25 volts. Finally the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power fail detection has occurred. Power fail detection also has the same effect on data transfer as the $\overline{RESET}$ input.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1

	7	6	5	4	3	2	1	0	HEX VALUE
Byte 0	1	1	0	0	0	1	0	1	C5
Byte 1	0	0	1	1	1	0	1	0	3A
Byte 2	1	0	1	0	0	0	1	1	A3
Byte 3	0	1	0	1	1	1	0	0	5C
Byte 4	1	1	0	0	0	1	0	1	C5
Byte 5	0	0	1	1	1	0	1	0	3A
Byte 6	1	0	1	0	0	0	1	1	A3
Byte 7	0	1	0	1	1	1	0	0	5C

NOTE:
The pattern recognition sequence in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the timekeeper is less than 1 in 10^{19}.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2

Register	7	6	5	4	3	2	1	0	Range (BCD)
0	0.1 SEC				0.01 SEC				00-99
1	0	10 SEC			SECONDS				00-59
2	0	10 MIN			MINUTES				00-59
3	12/24	0	10 / A/P	HR	HOUR				01-12 00-23
4	0	0	$\overline{\text{OSC}}$	$\overline{\text{RST}}$	0	DAY			01-07
5	0	0	10 DATE		DATE				01-31
6	0	0	0	10 MONTH	MONTH				01-12
7	10 YEAR				YEAR				00-99

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to 70°C
Soldering Temperature	260°C for 10 Sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1,3
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1,6
Logic 0	V_{IL}	−0.3		+0.8	V	1,6

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Current	I_{CC}			5	mA	3,4
Input Leakage	I_{IL}	−1.0		+1.0	uA	4,6
Output @2.4V	I_{OH}	−1.0			mA	2
Output @0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

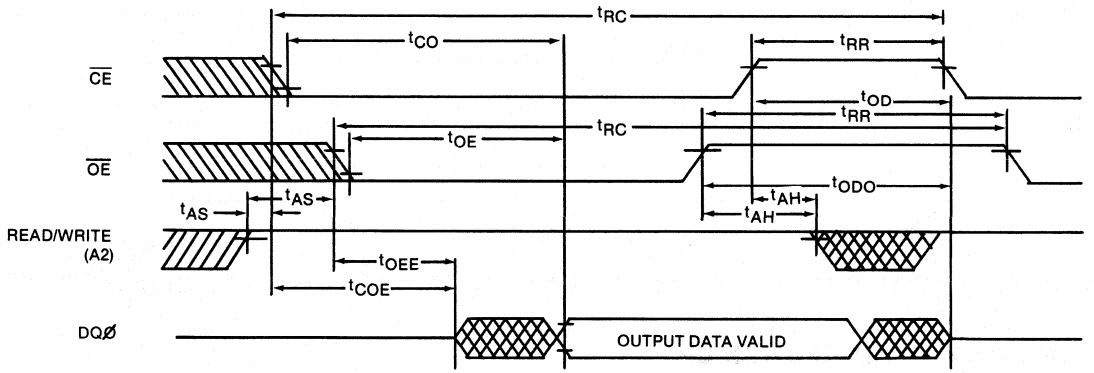
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			200	ns	
$\overline{CE}$ to Output in Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output in High Z	t_{OD}			100	ns	
$\overline{OE}$ to Output in High Z	t_{ODO}			100	ns	
Address Set Up Time	t_{AS}	20			ns	8
Address Hold Time	t_{AH}			10	ns	8
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
$\overline{OE}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	7
Data Set Up Time	t_{DS}	100			ns	8
Data Hold Time	t_{DH}	10			ns	8
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

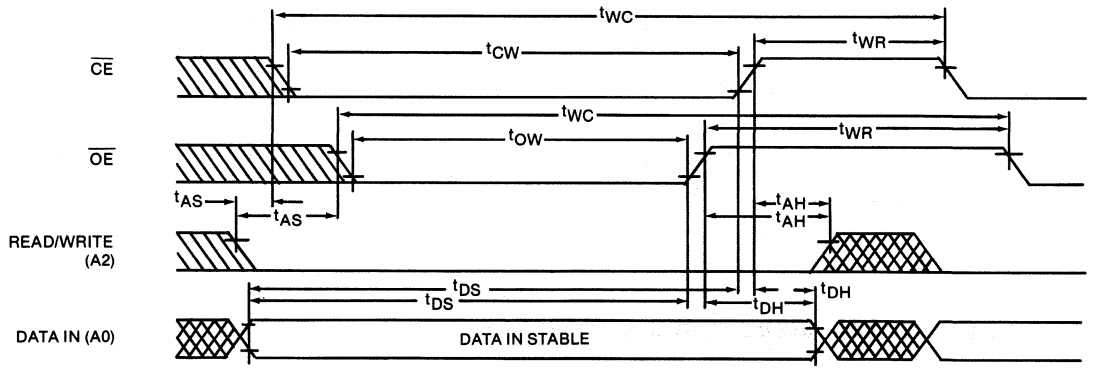
(0 °C to 70 °C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 -3V	t_F	0			ms	

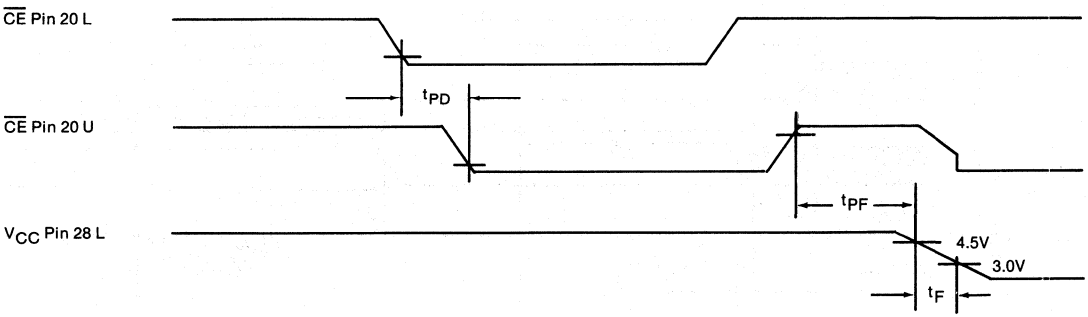
TIMING DIAGRAM— READ CYCLE



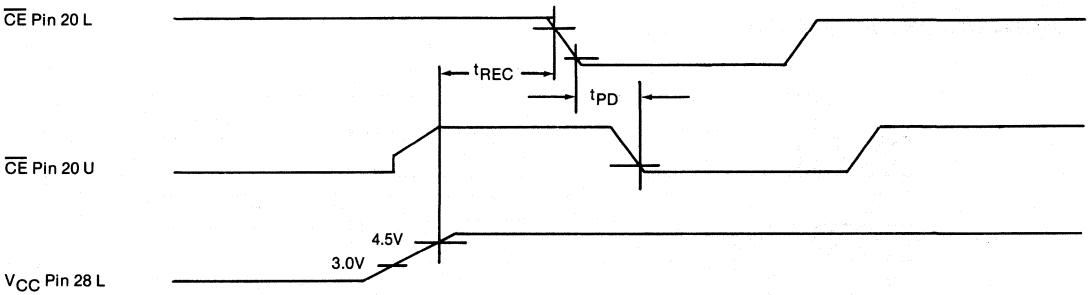
TIMING DIAGRAM—WRITE CYCLE



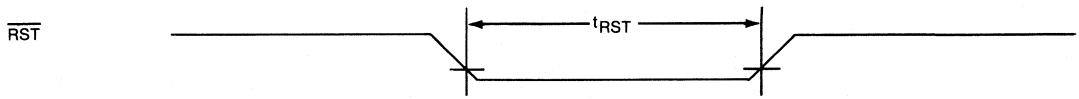
TIMING DIAGRAM— POWER DOWN



TIMING DIAGRAM— POWER UP



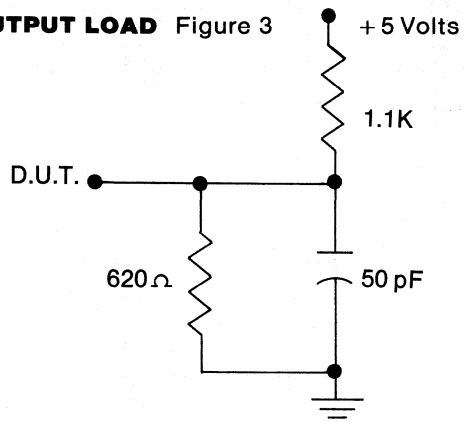
TIMING DIAGRAM—RESET FOR SMARTWATCH

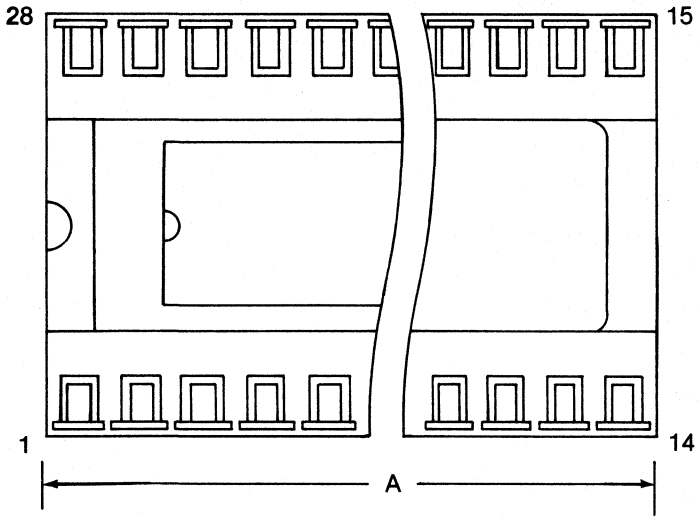


NOTES:

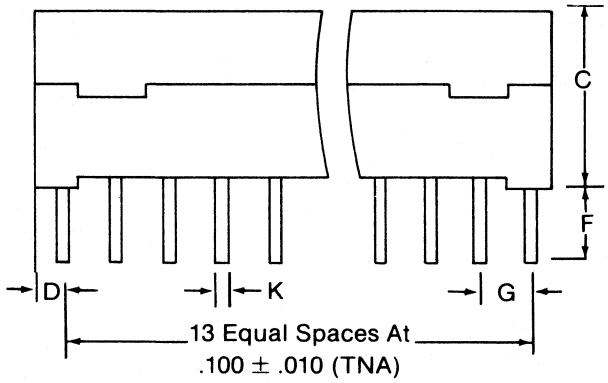
1. All voltages are referenced to ground.
2. Measured with a load shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Input pulse rise and fall times equal 10 ns.
6. Applies to Pins 1 L, 8 L, 10 L, 20 L, and 22 L.
7. t_{WR} and t_{RR} are functions of the latter occurring edge of $\overline{OE}$ or $\overline{CE}$.
8. t_{AS}, t_{AH}, t_{DS} and t_{DH} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.

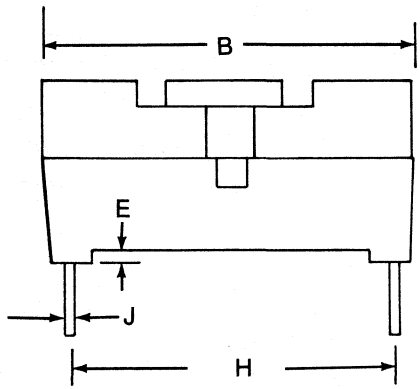
OUTPUT LOAD Figure 3





DIM.	INCHES	
	MIN.	MAX.
A	1.390	1.420
B	.695	.705
C	.350	.370
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.625
J	.008	.012
K	.015	.021





Dallas Semiconductor
Nonvolatile Read/Write Cartridge — *DS1217A*

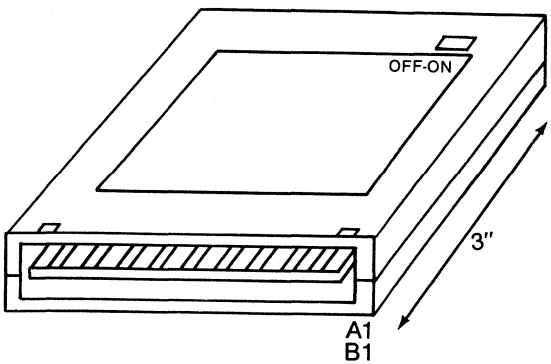
FEATURES

- User insertable
- Capacity up to 32K x 8
- Standard Bytewide pinout facilitates connection to JEDEC 28 pin DIP via ribbon cable
- Data retention greater than 10 years
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C
- Unauthorized access can be prevented with optional security feature

SIGNAL CONNECTIONS

Name	Position		Name
Ground	A1	B1	$\overline{\text{RESET}}$
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data (DQ0)
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground

PACKAGE



DESCRIPTION

The DS1217A is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge is available in density ranges from 2K × 8 to 32K × 8 in 8K-byte increments. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a 28-conductor ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin Bytewide memory sites.

The DS1217A cartridge has a lifetime energy source to retain data and circuitry needed to automatically protect memory content. Reading and writing the memory locations is the same as using conventional static RAM. If the user wants to convert from read/write memory to read-only memory, a manual switch is provided to unconditionally protect memory content.

READ MODE

The DS1217A is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217A is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217A constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217A checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217A provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28-pin Bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 499284-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin ribbon cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push out may occur as the distance between the cartridge and driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	UNUSED ADDRESS INPUTS
DS1217A/16K-25	2K x 8	*ADDRESS 11, 12, 13, 14
DS1217A/64K-25	8K x 8	ADDRESS 13, 14
DS1217A/128K-25	16K x 8	ADDRESS 14
DS1217A/192K-25	24K x 8	
DS1217A/256K-25	32K x 8	

*Unused address inputs must be held low (V_{IL}).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground $-0.3V$ to $+7.0V$
Operating Temperature 0°C to 70°C
Storage Temperature $-40°C$ to $+70°C$

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		+0.8	V

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	−60		+60	*u*A
I/O Leakage Current	I_{LO}	−10		+10	*u*A
Output Current @2.4V	I_{OH}	−1.0	−2.0		mA
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA
Standby Current $\overline{CE}=2.2V$	I_{CC}	5.0		10	mA
Operating Current	I_{CC}			75	mA

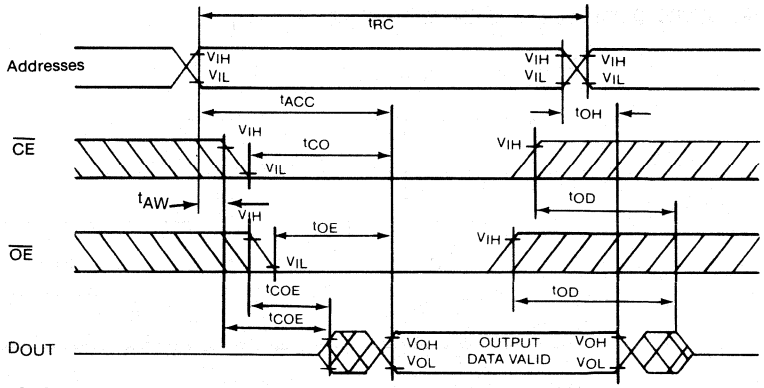
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	75	pF	
Input/Output Capacitance	$C_{I/O}$	75	pF	

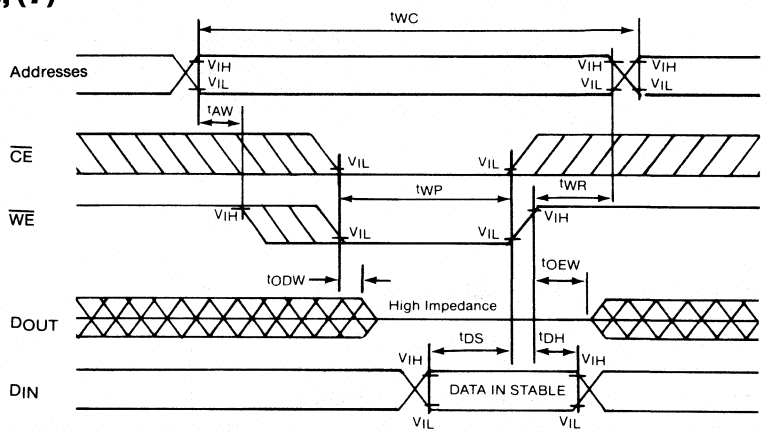
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			250	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10			ns	
Output High Z From Deselection	t_{OD}			125	ns	
Output Hold From Address Change	t_{OH}	10			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Set Up Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z From $\overline{WE}$	t_{ODW}			100	ns	
Output Active From $\overline{WE}$	t_{OEW}	10			ns	
Data Set Up Time	t_{DS}	100			ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	0			ns	4,5

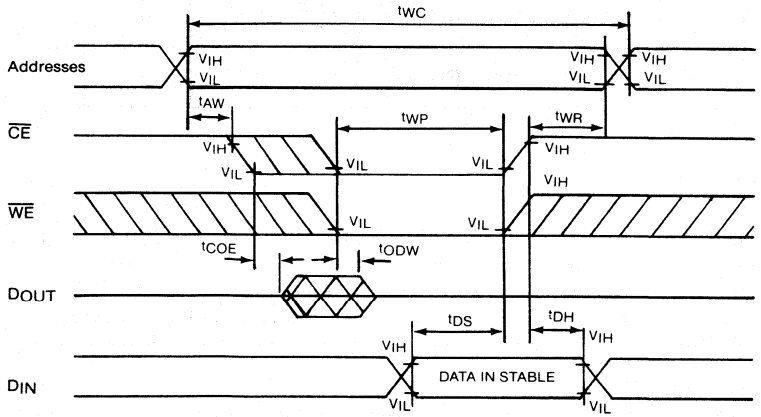
READ CYCLE (1)



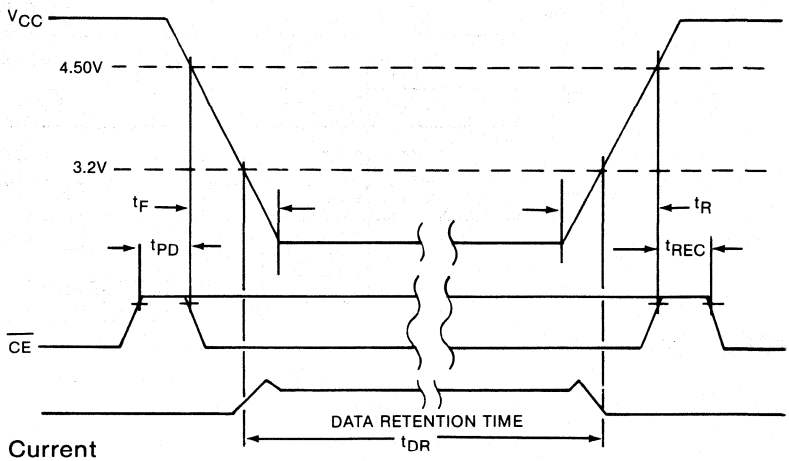
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	10
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	2	125	ms	10

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1217A is market with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

D.C. Test Conditions
Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

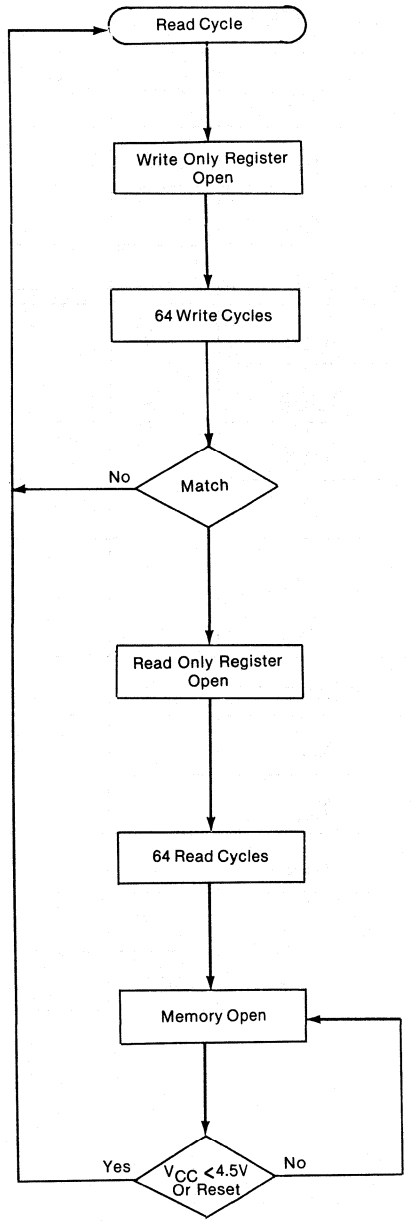
A.C. Test Conditions
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 1). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1217A using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the cartridge without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1217A by Dallas Semiconductor at time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1217A and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1217A by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register may be used by software to determine if the cartridge will be permitted to be used with that particular system. After the 64th read cycle has been executed the cartridge is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V_{CC} falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.
Note: Contact Dallas Semiconductor sales office for code assignment.

SECURITY SEQUENCE

Figure 1



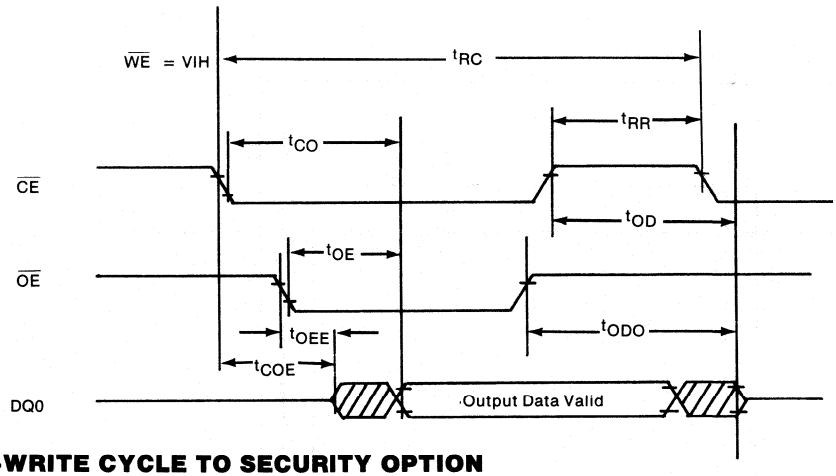
SECURITY OPTION

A.C. ELECTRICAL CHARACTERISTICS

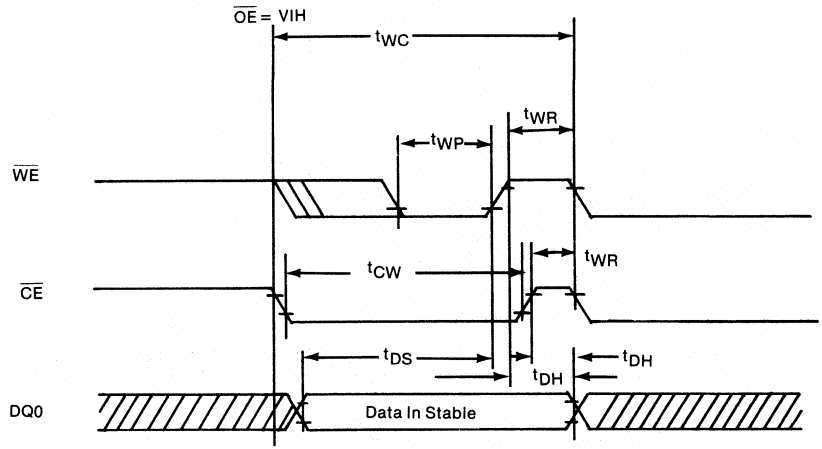
(0 °C - 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Read Cycle Time	t_{RC}	250			ns
$\overline{CE}$ Access Time	t_{CO}			200	ns
$\overline{OE}$ Access Time	t_{OE}			100	ns
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns
$\overline{CE}$ To Output High Z	t_{OD}			100	ns
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns
Read Recovery	t_{RR}	50			ns
Write Cycle	t_{WC}	250			ns
Write Pulse Width	t_{WP}	170			ns
Write Recovery	t_{WR}	50			ns
Data Set Up	t_{DS}	100			ns
Data Hold Time	t_{DH}	0			ns
$\overline{CE}$ Pulse Width	t_{CW}	170			ns
Reset Pulse Width	t_{RST}	200			ns

TIMING DIAGRAM—READ CYCLE TO SECURITY OPTION



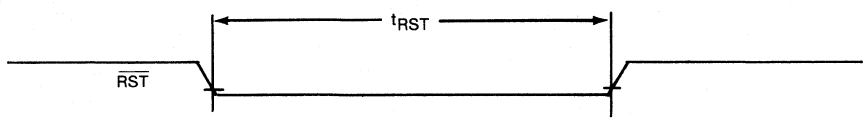
TIMING DIAGRAM—WRITE CYCLE TO SECURITY OPTION



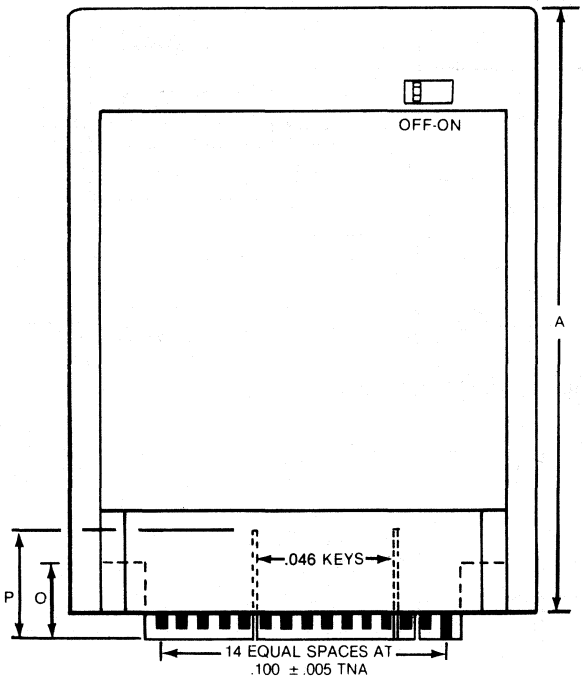
NOTES:

1. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

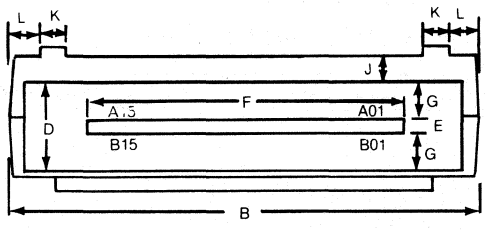
TIMING DIAGRAM—RESET FOR SECURITY OPTION

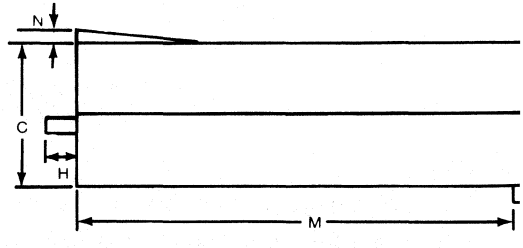


Nonvolatile Read/Write Cartridge
DS1217A



DIM.	INCHES	
	MIN.	MAX
A	3.020	3.040
B	2.280	2.300
C	.590	.610
D	.440	.460
E	.060	.065
F	1.590	1.607
G	.190	.200
H	.115	.135
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060
O	.039	.405
P	.405	.425





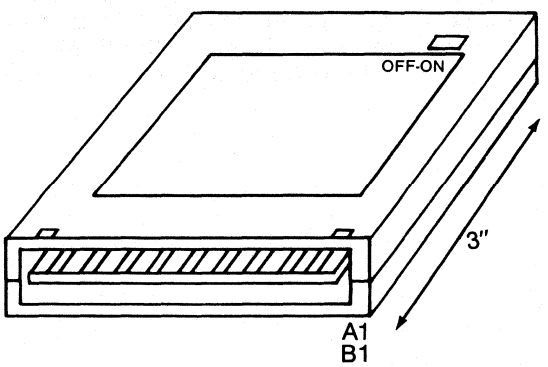
Dallas Semiconductor
Nonvolatile Read/Write Cartridge

PRELIMINARY
DS1217M

FEATURES

- User insertable
- Data retention greater than 10 years
- Capacity up to 512K x 8
- Standard Bytewide pinout facilitates connection to JEDEC 28 pin DIP via ribbon cable
- Software controlled banks maintain 32K x 8 JEDEC 28 pin compatability
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C

PACKAGE



SIGNAL CONNECTIONS

NAME	POSITION		NAME
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 2
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground

DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 64K × 8 to 512K × 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30 pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28 pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28 Pin bytewide memory sites.

READ MODE

The DS1217M is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217M is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217M constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217M provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

BANK SWITCHING

Bank switching is accomplished via address lines A8, A9, A10 and A11. Initially, on power up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64 bit pattern which will set the bank switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 4 bits. Each set of address inputs are entered into the DS1217M by executing read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10 and A11. However, address line 8 defines which of the 16 banks that is to be enabled, or all banks deselected, as per Table 3.

Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch data sheet for more detail.)

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28 pin Bytewide sockets can be retrofitted using a 28 pin DIP plug. The DIP plug, AMP Part Number 499284-2, can be inserted into the 28 pin site after the memory is removed. Connection to the cartridge is accomplished via a 28 pin cable connected to a 30 contact card edge connector, AMP Part Number 499188-4. The 28 pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push out may occur as the distance between the cartridge and the driving circuitry is increased.

TABLE 1 — CARTRIDGE NUMBERING

PART NO.	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64K x 8	2
DS1217M 1-25	128K x 8	4
*DS1217M 2-25	256K x 8	8
*DS1217M 3-25	384K x 8	12
*DS1217M 4-25	512K x 8	16

*Contact Dallas Semiconductor sales offices for availability

TABLE 2 — ADDRESS INPUT PATTERN

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A_8	1	0	1	0	0	0	1	1	0	1	0	X	X	X	X	X
A_9	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_{10}	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_{11}	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

TABLE 3 — BANK SELECT TABLE

BANK SELECTED	A_8 BIT SEQUENCE				
	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	1	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1	0	0	1	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0
BANK 7	1	0	1	1	1
BANK 8	1	1	0	0	0
BANK 9	1	1	0	0	1
BANK 10	1	1	0	1	0
BANK 11	1	1	0	1	1
BANK 12	1	1	1	0	0
BANK 13	1	1	1	0	1
BANK 14	1	1	1	1	0
BANK 15	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		+0.8	V

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	−60		+60	uA
I/O Leakage Current	I_{LO}	−10		+10	uA
Output Current @2.4V	I_{OH}	−1.0	−2.0		mA
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA
Standby Current $\overline{CE}=2.2V$	I_{CC}			25	mA
Operating Current	I_{CC}			75	mA

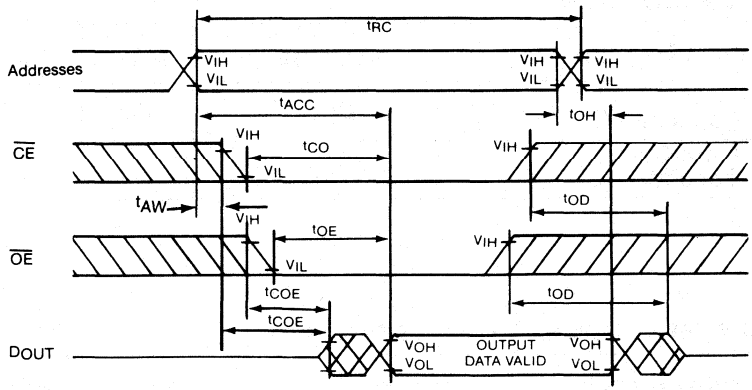
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	100	pF	
Input/Output Capacitance	C_{OUT}	100	pF	

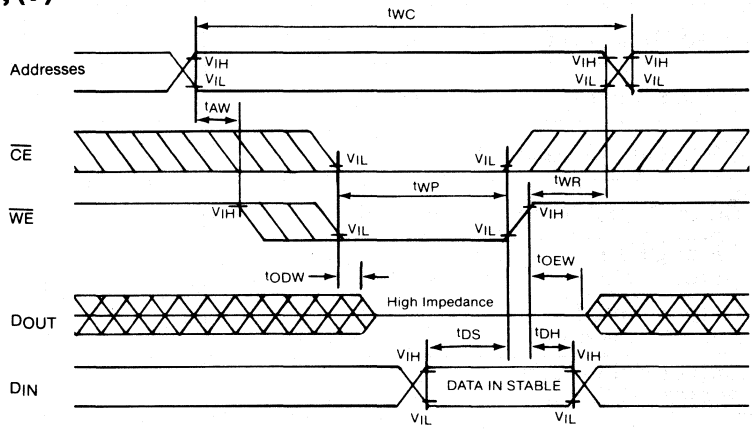
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			210	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			210	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10			ns	
Output High Z From Deselection	t_{OD}			125	ns	
Output Hold From Address Change	t_{OH}	10			ns	
Read Recovery Time	t_{RR}	40		ns		
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Set Up Time	t_{AW}	0		ns		
Write Recovery Time	t_{WR}	20			ns	
Output High Z From $\overline{WE}$	t_{ODW}			100	ns	
Output Active From $\overline{WE}$	t_{OEW}	10			ns	
Data Set Up Time	t_{DS}	100			ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	0			ns	4,5

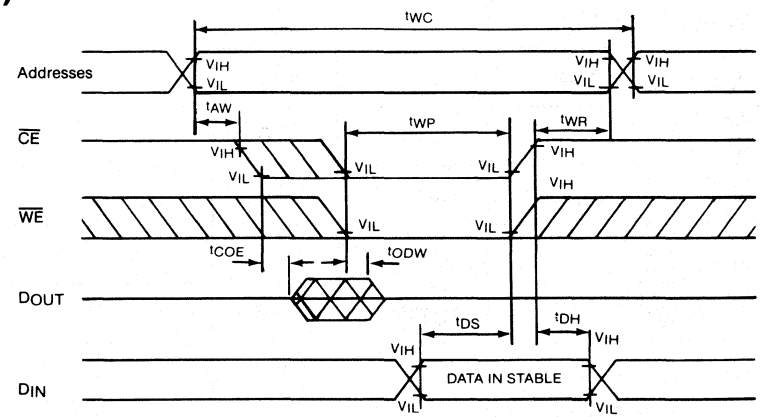
READ CYCLE (1)



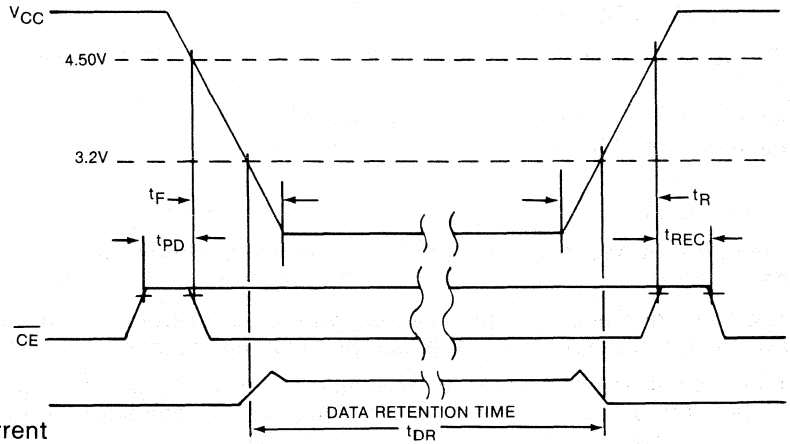
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	10
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	2	125	ms	10

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

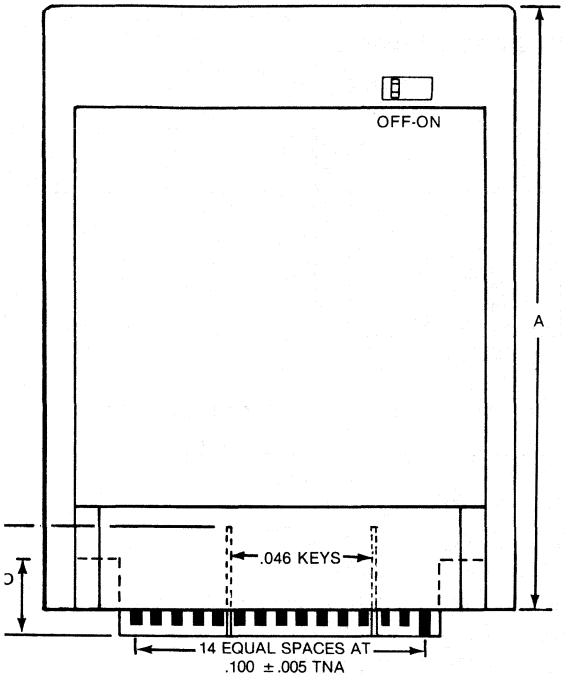
NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20ns$.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1217M is market with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

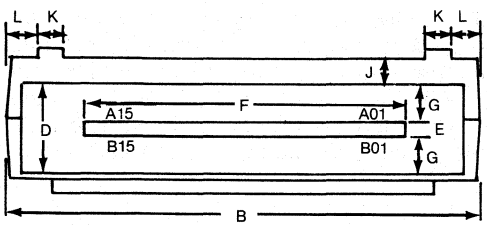
D.C. Test Conditions
Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

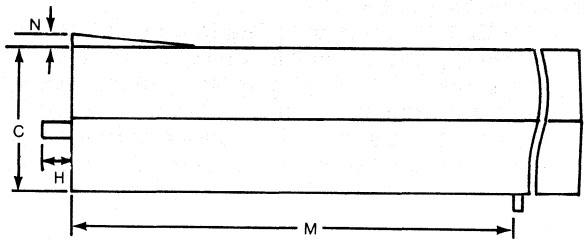
A.C. Test Conditions
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

Nonvolatile Read/Write Cartridge
DS1217M



DIM.	INCHES	
	MIN.	MAX.
A	3.020	3.040
B	2.280	2.300
C	.590	.610
D	.440	.460
E	.060	.065
F	1.590	1.607
G	.190	.200
H	.115	.135
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060
O	.039	.405
P	.405	.425





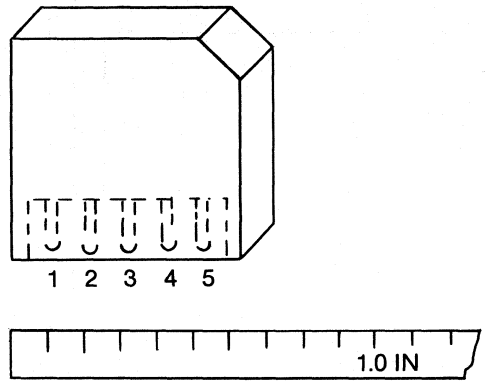
Dallas Semiconductor
Electronic Tag

DS1201

FEATURES

- User insertable
- Nonvolatile—greater than 10 years of data retention
- 1024 bits of read/write memory
- Miniature and transportable
- Durable and rugged
- Impervious to handling
- 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Low power CMOS circuitry
- Applications include software authorization, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record

PIN CONNECTIONS



PIN NAMES

Pin 1 — V_{CC}	+5 VOLTS
Pin 2 — $\overline{RST}$	$\overline{RESET}$
Pin 3 — DQ	DATA INPUT/OUTPUT
Pin 4 — CLK	CLOCK
Pin 5 — GND	GROUND

DESCRIPTION

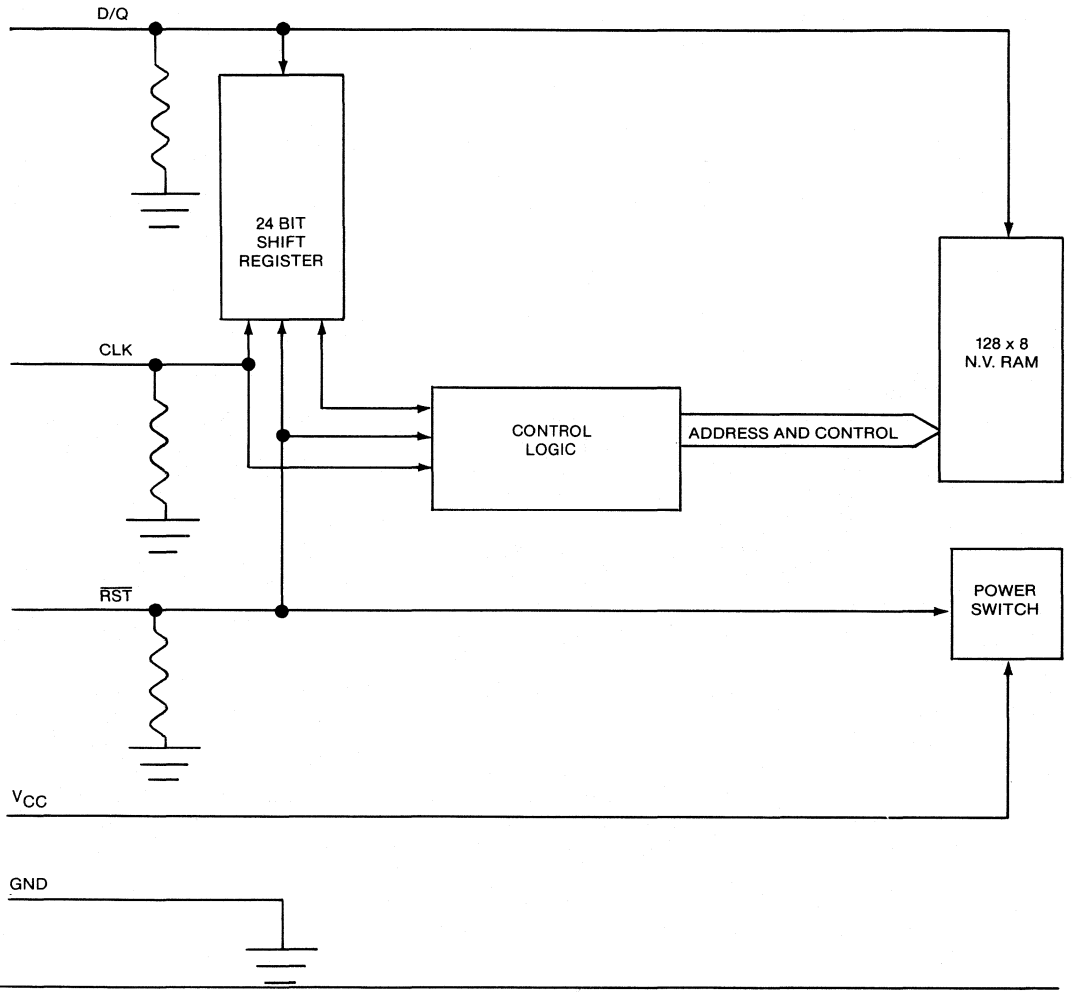
The DS1201 Electronic Tag is a miniature nonvolatile, read/write memory system which can randomly access individual 8-bit strings (bytes) or sequentialy access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user.

OPERATION

The block diagram (Figure 1) of the electronic tag illustrates the main elements of the device; namely, shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the shift register providing both address and command information. Each bit is serial input on the rising edge of the CLOCK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKs which load the shift register, additional CLOCKs will output data for a read, or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

The tag can be used as a four-pin or five-pin device, depending on the application. For hardwired aplications, active power is supplied by the V_{CC} pin. Alternatively, for user insertable applications, power can be supplied by the $\overline{\text{RESET}}$ pin.

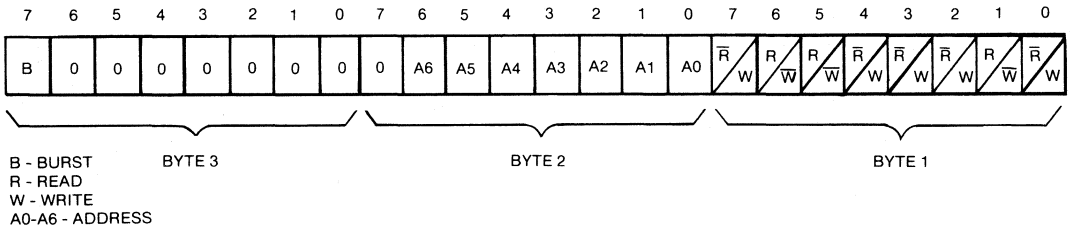
ELECTRONIC TAG BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND

Each memory transfer consists of a three-byte address/command input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address/command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logical 0. This bit is reserved for future higher density versions of the tag. If bit 7 does not equal logical 0, the cycle is aborted and all future inputs to the tag are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The third byte of the address/command is also set aside for future expansion. Bits 0 through 6 must be set to logical 0 or the cycle will be aborted and all future inputs are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. Bit 7 of byte three of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A7 equals logical 0 and bit 7 of byte three of the address/command equals logical 1, the tag will enter the burst mode after the address/command sequence is complete.

FIGURE 2



BURST MODE

Burst mode is specified for the electronic tag when all address bits (A0-A6) of the address/command are set to logical 0 and bit 7 of byte three to logical 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the $\overline{\text{RESET}}$ input is driven low.

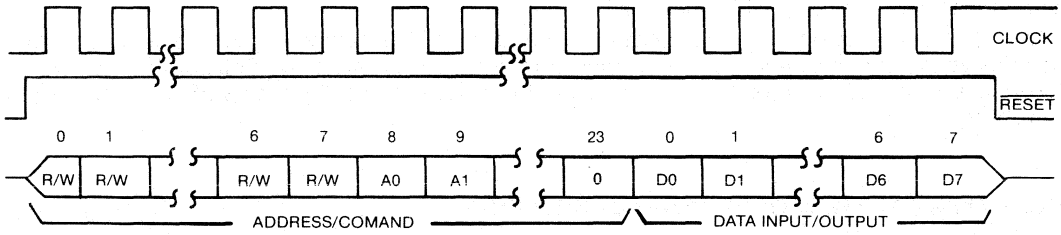
RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{\text{RESET}}$ input high. The $\overline{\text{RESET}}$ input serves three functions. First, $\overline{\text{RESET}}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{\text{RESET}}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{\text{RESET}}$ of 2 mA @ 3.8 volts is required. However, if the V_{CC} pin is connected to a 5 volt source within nominal limits, then $\overline{\text{RESET}}$ pin is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 *u*A. Finally, the $\overline{\text{RESET}}$ signal provides a method of terminating either single byte or multiple byte data transfers. A CLOCK cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of CLOCK cycle. Address/command bits and data bits are input on the rising edge of the CLOCK and data bits are output on the falling edge of the CLOCK. All data transfer terminates if the $\overline{\text{RESET}}$ input is low and D/Q pin goes to a high impedance state. When data transfer to the tag is terminated using reset, the transition of $\overline{\text{RESET}}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

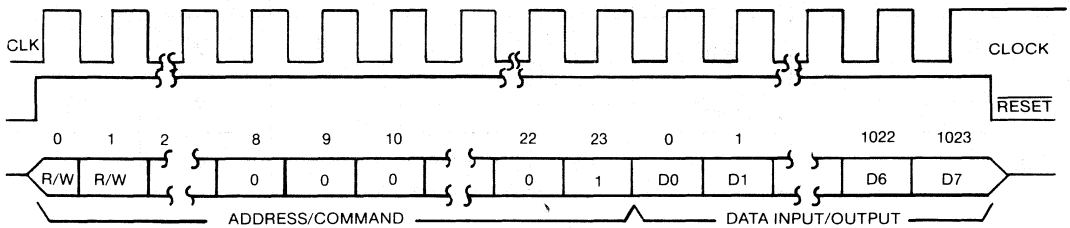
DATA TRANSFER

FIGURE 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



NOTES
1.) DATA INPUT SAMPLED ON RISING EDGE OF CLOCK
2.) DATA OUTPUT CHANGES ON FALLING EDGE OF CLOCK

DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

DATA OUTPUT

Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for the data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

TAG CONNECTIONS

The tag is designed to be plugged into a standard 5-pin, 0.1-inch-center SIP receptacle. A key is provided to prevent the tag from being plugged in backwards and to aid in alignment of the receptacle. For portable applications, contact to the tag pins can be determined to insure connection integrity before data transfer begins. CLOCK, $\overline{\text{RESET}}$, and DATA INPUT/OUTPUT all have internal 20K Ohm pull down resistors to ground which can be sensed by a reading device.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1,2,10
Logic 0	V_{IL}	-0.3		0.8	V	1
$\overline{\text{RESET}}$ Logic 1	V_{IHE}	3.8			V	1,7,11
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	μA	5
Output Leakage	I_{LO}			+500	μA	5
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input RESISTANCE	Z_{RST}	10		40	KΩ	1
D/Q Input RESISTANCE	Z_{DQ}	10		40	KΩ	1
CLK Input RESISTANCE	Z_{CLK}	10		40	KΩ	1
Active Current	I_{CC1}			6	mA	8
Standby Current	I_{CC2}			1	mA	8
$\overline{\text{RST}}$ Current	I_{RST}				mA	7,8,13

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS

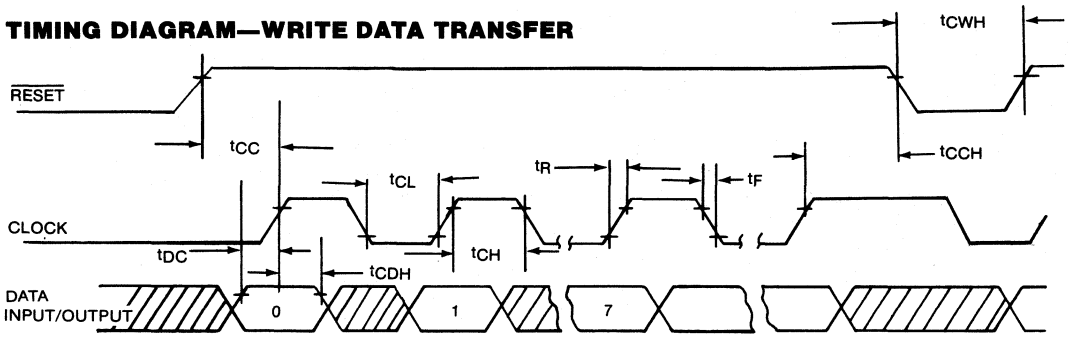
(0°C to 70°C, V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	35			ns	3,9
Data To CLK Hold	t_{CDH}	40			ns	3,9
Data To CLK Delay	t_{CDD}			125	ns	3,4,6,9
CLK Low Time	t_{CL}	125			ns	3,9
CLK High Time	t_{CH}	125			ns	3,9
CLK Frequency	f_{CLK}	D.C.		4.0	MHZ	3,9
CLK Rise & Fall	t_R,t_F			500	ns	9
$\overline{RST}$ To CLK Set Up	t_{CC}	1			μs	3, 9
CLK To $\overline{RST}$ Hold	t_{CCH}	40			ns	3,9
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	3,9,14
$\overline{RST}$ To I/O High Z	t_{CDZ}			50	ns	3,9

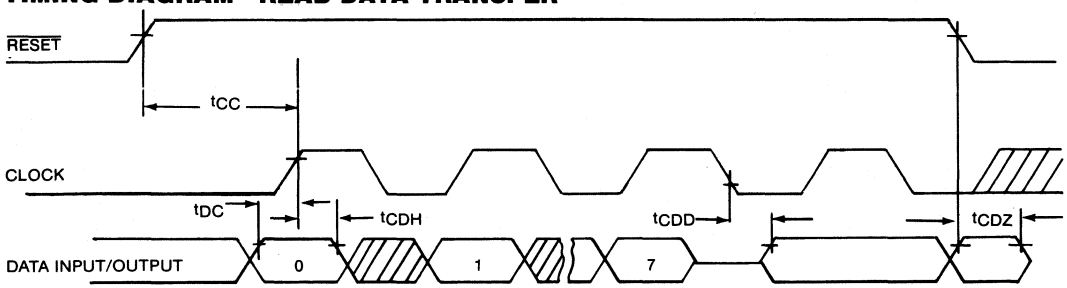
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	12

TIMING DIAGRAM—WRITE DATA TRANSFER



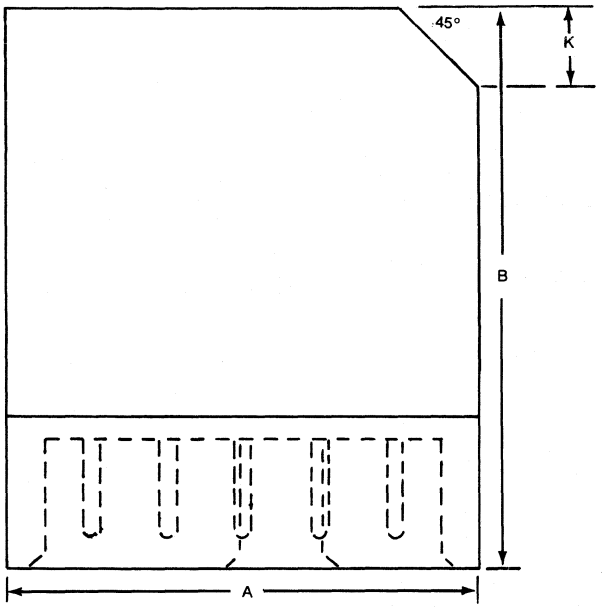
TIMING DIAGRAM—READ DATA TRANSFER



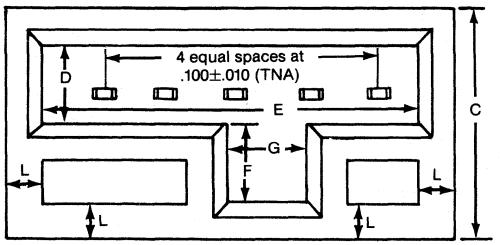
NOTES

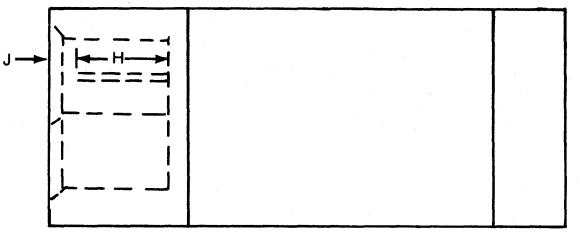
1. All voltages and resistances are referenced to GND.
2. Input levels apply to CLK, D/Q, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the tag, then the $\overline{RST}$ input reverts to V_{IHE}.
3. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
4. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
5. For CLK, D/Q, $\overline{RST}$, and V_{CC} at 5 volts.
6. Load capacitance = 50 pF.
7. Applies to $\overline{RST}$ when $V_{CC} < 3.8$ V.
8. Measured with outputs open.
9. Measured at V_{IH} of $\overline{RST} \geq 3.8V$ when $\overline{RST}$ supplies power.
10. Logic 1 maximum is $V_{CC} + 0.3$ volts if the V_{CC} pin supplies power and $\overline{RST} + 0.3$ volts if the $\overline{RST}$ pin supplies power.
11. $\overline{RST}$ logic 1 maximum is $V_{CC} + 0.3$ volts if the V_{CC} pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1201 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average A.C. $\overline{RST}$ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ D.C.} + (4 \times 10^{-3})(C_L + 140) f$
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHZ.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHZ gives an I_{TOTAL} current of 5 mA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to 100 ms.

Electronic Tag
DS1201



DIM.	INCHES	
	MIN.	MAX.
A	.610	.625
B	.745	.755
C	.310	.320
D	.100	.110
E	.515	.525
F	.100	.110
G	.100	.110
H	.110	.130
J	.030	.050
K	.045	.055
L	.045	.055





Dallas Semiconductor
KeyRing

DS1250

FEATURES

- Low cost add-on fixture for Electronic Keys and Tags
- No hardware changes needed to retrofit existing systems
- Layman installation
- Normal system operation unaffected
- Key or Tag communication totally controlled by software
- Typical 50 K bits/s communication rate
- Up to 5 Keys and/or Tags resident at one time

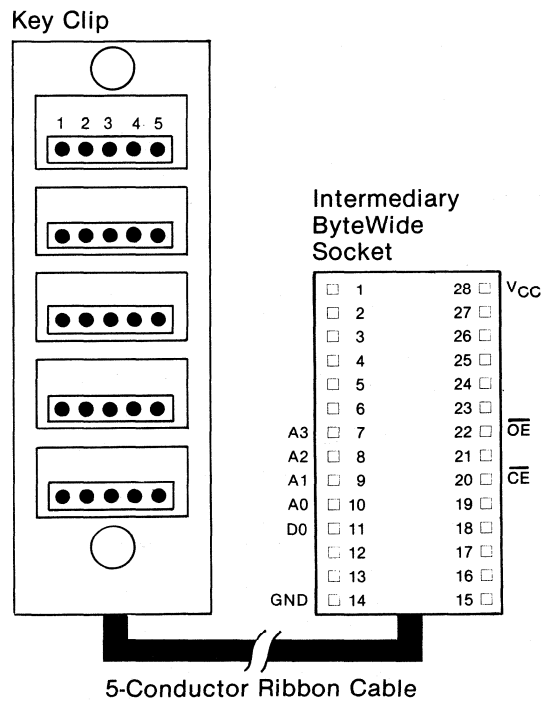
PIN CONNECTIONS AND DEFINITIONS

Intermediary ByteWide Socket
Pins 7-10 - Address Inputs
Pin 11 - D0
Pin 20 - conditioned Chip Enable
Pin 22 - Output Enable
Pin 14 - Ground
Pin 28 - V_{CC}

All pins pass through except 20

Key Clip

Pin 1 - V_{CC} +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - DQ - Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND - Ground



DESCRIPTION

The DS1250 KeyRing adapts low pin count Electronic Keys (DS1204) or Tags (DS1201) to JEDEC ByteWide memory signals without affecting system operation. A simple, layman procedure is all that is needed to retrofit an existing system. Any 28 pin RAM, ROM, or EPROM can be removed, placed in the intermediary socket, and then reinstalled in the original location leaving the system intact. The emanating 5 conductor ribbon cable can be routed out of the system enclosure if desired and the clip can be attached where convenient with the adhesive provided. Up to 5 Keys and/or Tags can be inserted in the clip at the same time. The intermediary socket contains a CMOS integrated circuit which redirects information flow from the ByteWide memory to the inserted Keys/Tags. A special software generated address sequence causes the redirection to take place. Typical data transfer rates of 50 K bits/s are possible with an assembly language software driver.

HARDWARE IMPLEMENTATION 28-PIN ROM SOCKET

Bytewide KeyRing application begins with a system board which contains a 28-pin socket with or without a ROM contained in the socket. In most system implementations and all PCs, there is at least one ROM which is used for boot sequences, basic I/O system implementation, EPROM storage, or some form of dedicated software monitor application.

Installation of the Bytewide KeyRing requires the removal of the existing 28-pin ROM and the insertion of the Bytewide KeyRing socket pins into the system board socket. After this is accomplished, the original ROM is reinserted into the socket at the top of the Bytewide KeyRing. Then the five-conductor ribbon cable which connects the clip to the Bytewide socket is routed to the outside of the computer cabinet. Finally the clip can be attached to a convenient place on the computer cabinet using the supplied adhesive.

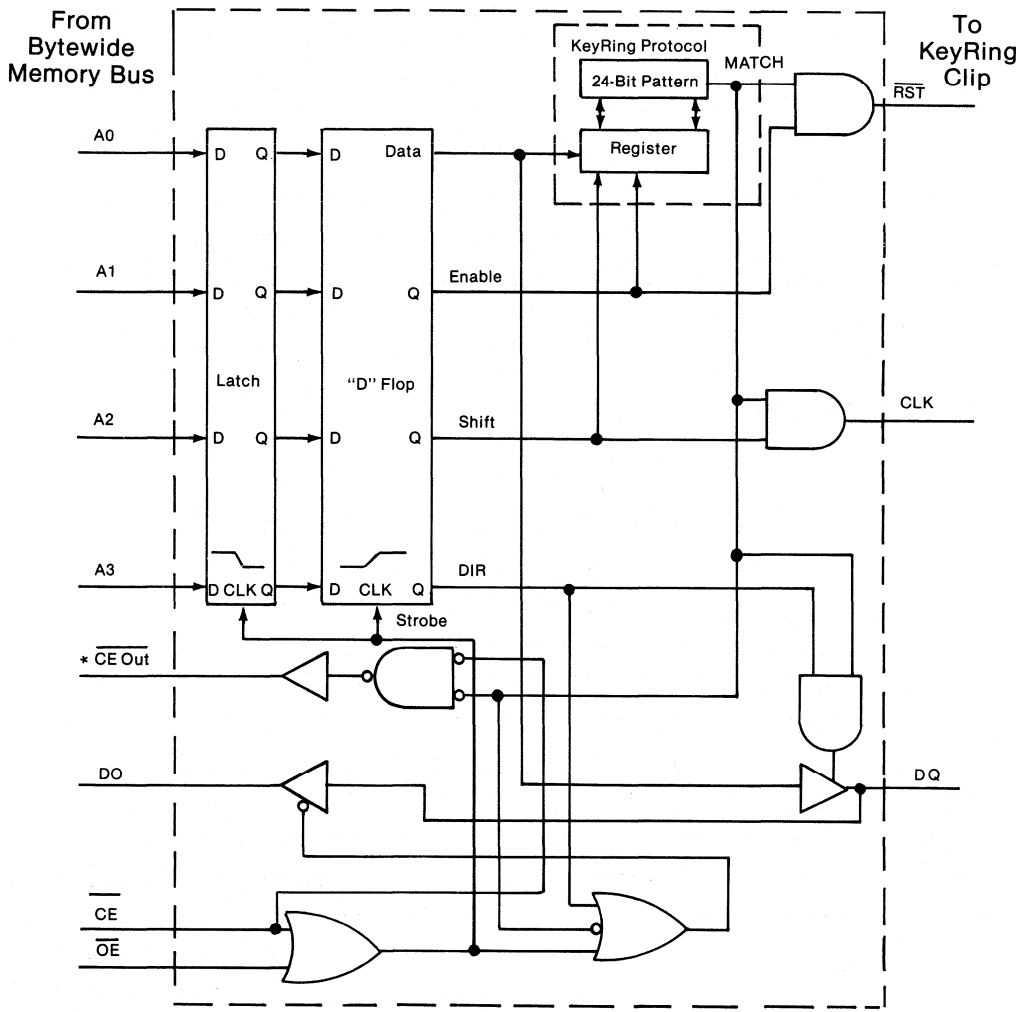
Under normal conditions, the system ROM will function as before, with address and data lines being transparently ported through the Bytewide KeyRing socket and presented to the system ROM as in the original configuration. As a result, existing non-Key-protected software will run on the system unaffected. However, if certain address lines are probed with specific patterns under software control, the KeyRing is activated and the system ROM becomes electrically disconnected from the system board. Instead, the address and data bus become electrically tied to the KeyRing bus. At this point, communication to the system board ROM socket is passed on transparently to any device(s) which are inserted into the KeyRing clip.

KEYRING OPERATION

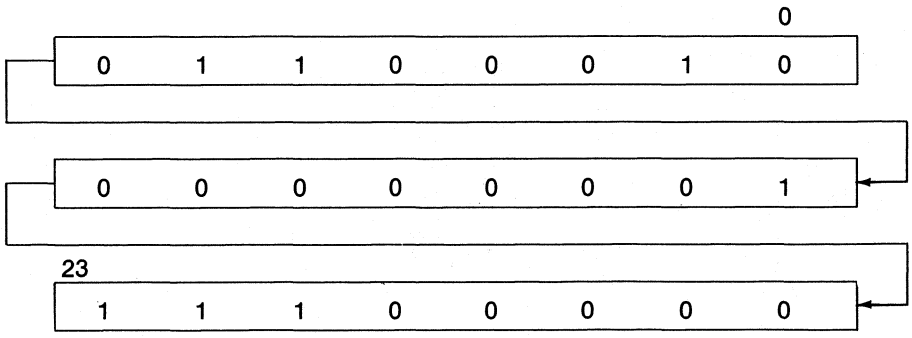
The main parts of the KeyRing are shown in the block diagram of Figure 1. Information presented on address inputs of the ROM are latched into the KeyRing on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}$ In and $\overline{OE}$ In. The $\overline{CE}$ input is connected to the memory bus $\overline{CE}$ and the $\overline{OE}$ input is connected to the memory bus $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit KeyRing protocol and to logic which will generate signals for Keys and Tags. The KeyRing protocol is derived from address inputs A0, A1 and A2. A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable communications. A1 must remain high during the pattern recognition sequence and subsequent communications with Keys after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and access is denied.

Data transfer through the KeyRing occurs by matching a 24-bit pattern, as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Therefore, data is input for comparison to the KeyRing protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the same level for both memory cycles. Address input A3 is used to control the direction of data going to and from Keys. This input is not used during pattern recognition of the KeyRing protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for Keys. The match signal is also used to disable Chip Enable to the topside memory and enable a gate which allows Key DQ to drive D0 line to the memory bus. When $\overline{RST}$ is driven high, devices attached to the KeyRing become active. Subsequent shift signals derived from A2 will now be recognized as the Key clock. The data signal for the Key is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on Key DQ. When A3 is set low, devices attached to the KeyRing can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the Key DQ.

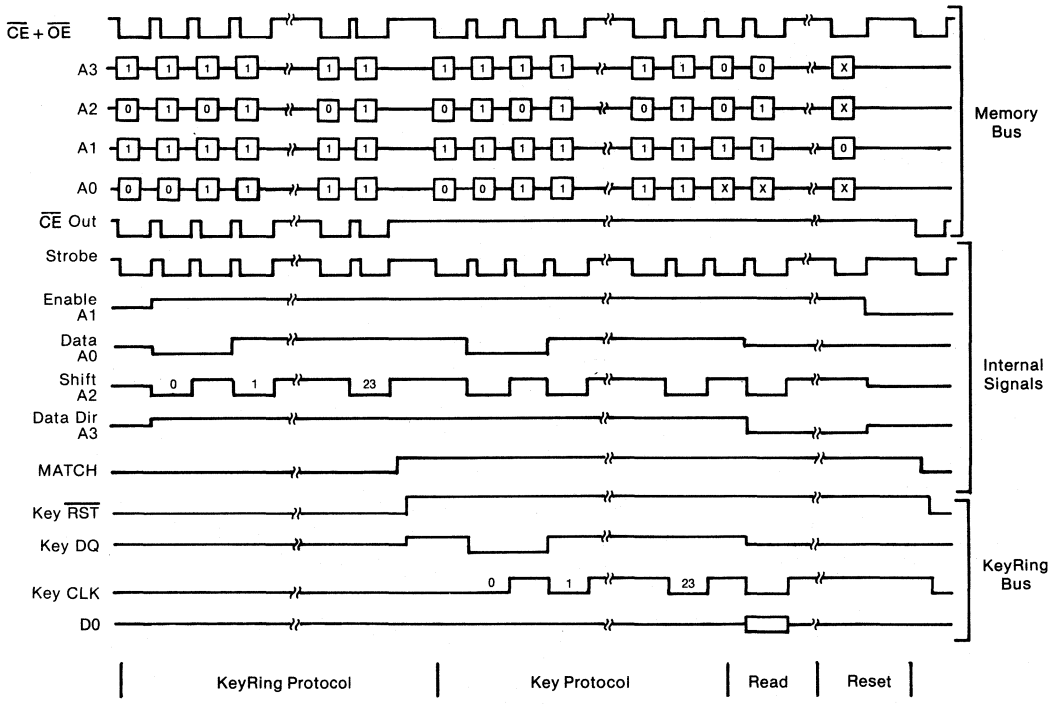
KEYRING BLOCK DIAGRAM Figure 1



KEYRING PROTOCOL Figure 2



KEYRING SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1		1	*u*A	
Output Leakage	I_{LO}			1	*u*A	
Output Current @2.4V	I_{OH}	−1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

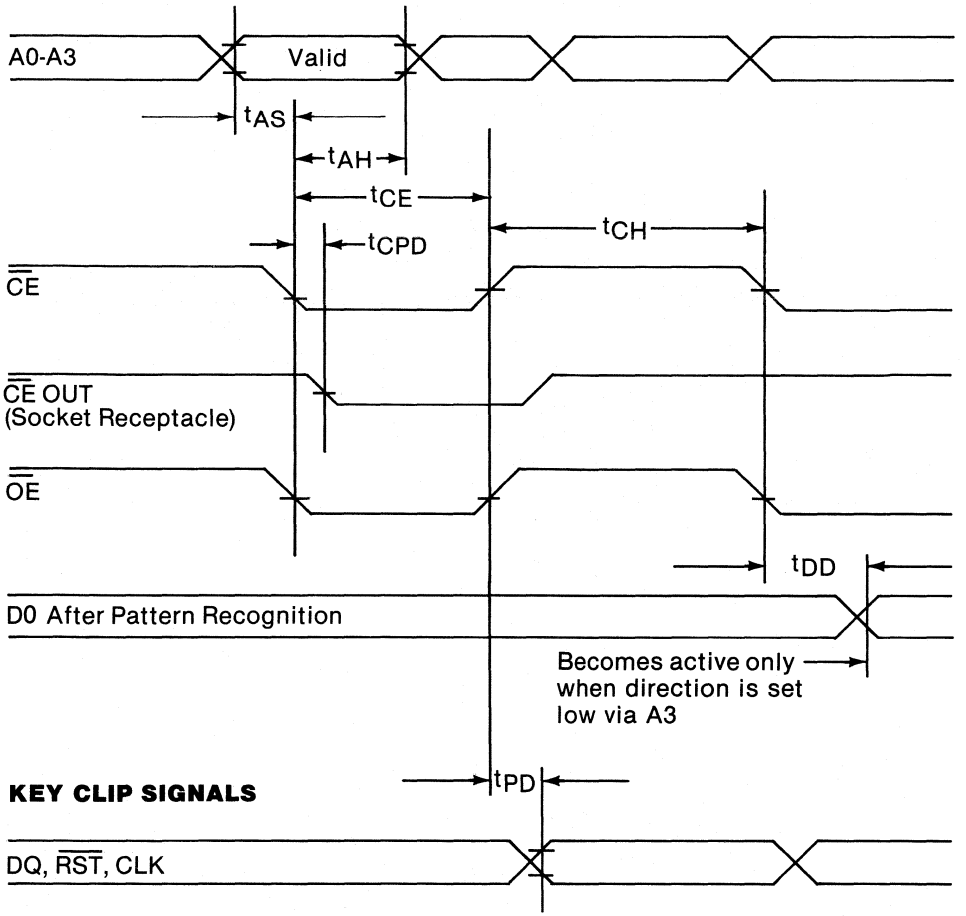
CAPACITANCE ($t_A = 25\,°C$)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output	$C_{I/O}$	5	10	pF	

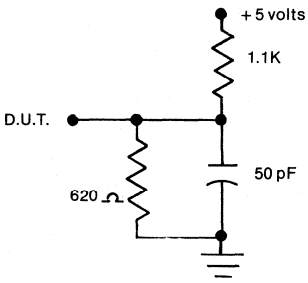
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Set Up	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	
$\overline{CE}$ Propagation Delay	t_{CPD}			10	ns	

BYTEWIDE MEMORY BUS



OUTPUT LOAD Figure 4



NOTES:

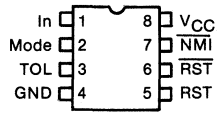
1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

Dallas Semiconductor
Power Monitor

DS1231-20
-35
-50

FEATURES
- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying non-volatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V_{CC} monitoring
- Replaces power up reset circuitry
- No external capacitors required

PIN CONNECTIONS



PIN NAMES

Pin 1	- In	Input
Pin 2	- Mode	Selects input pin characteristics
Pin 3	- TOL	Selects 5% or 10% V_{CC} detect
Pin 4	- GND	Ground
Pin 5	- RST	Reset (Active High)
Pin 6	- $\overline{RST}$	$\overline{Reset}$ (Active Low, open drain)
Pin 7	- $\overline{NMI}$	Nonmaskable interrupt
Pin 8	- V_{CC}	Power

DESCRIPTION
The DS1231 Power Monitor uses a precise temperature compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required, a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the power monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V_{CC} falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

OPERATION

The DS1231 Power Monitor provides the function of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring V_{CC} (Pin 8). The V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6) when V_{CC} falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and $\overline{RST}$ signals will become active as V_{CC} goes below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} goes below 4.5 volts. The RST and $\overline{RST}$ signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the $\overline{NMI}$ signal (Pin 7) when the input threshold voltage (VTP) falls to a level as determined by mode (Pin 2). When the mode pin is connected to V_{CC}, detection occurs at VTP−. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the mode pin is connected to ground, detection occurs at VTP+. In this mode Pin 1 sources 30 uA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between $\overline{NMI}$ and $\overline{RST}$. On power up, $\overline{NMI}$ is released as soon as the input threshold voltage (VTP) is achieved and V_{CC} is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

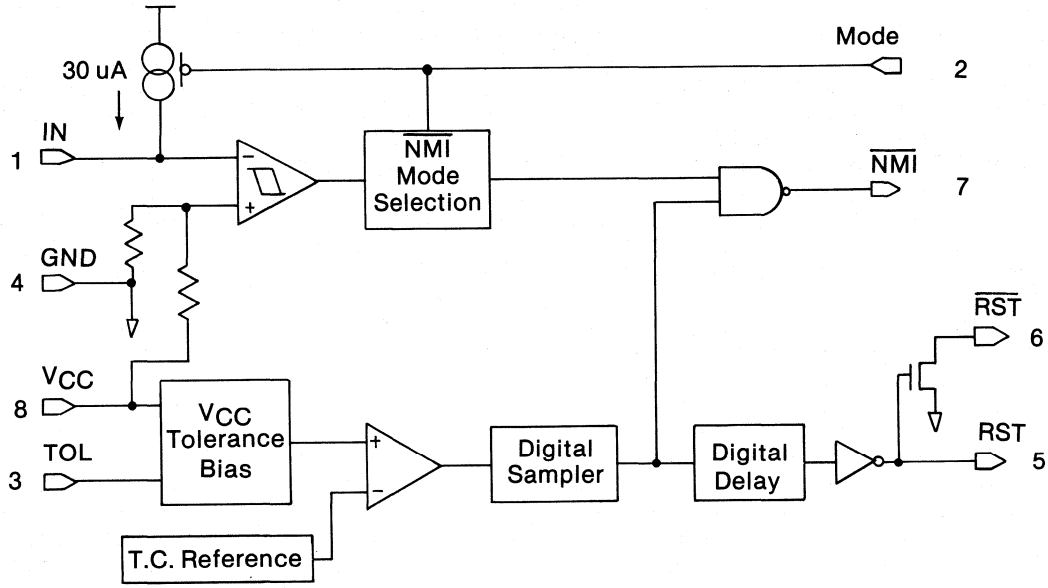
APPLICATION—MODE PIN CONNECTED TO V_{CC}

When the mode pin is connected to V_{CC}, Pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

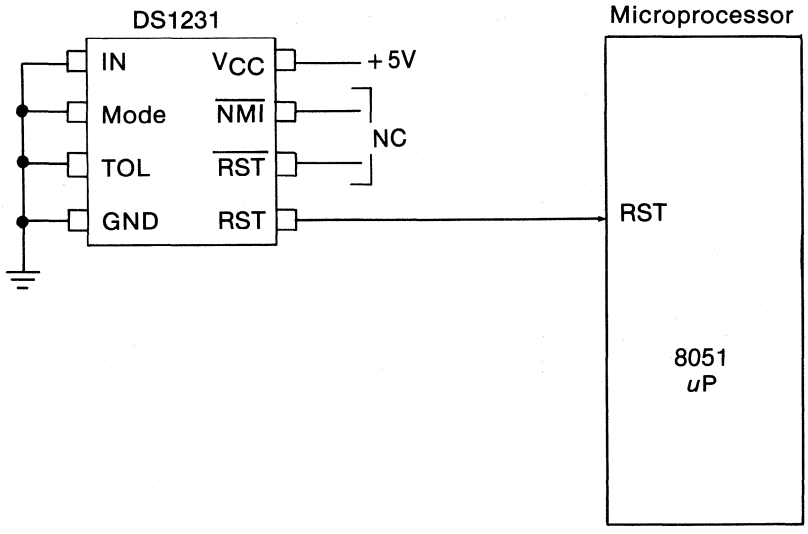
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1) which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point VTP− is 2.3 volts (using the −20 device), and the maximum allowable voltage on Pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0 = .46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate $\overline{NMI}$.

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high impedance to keep power consumption low and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to V_{CC}.

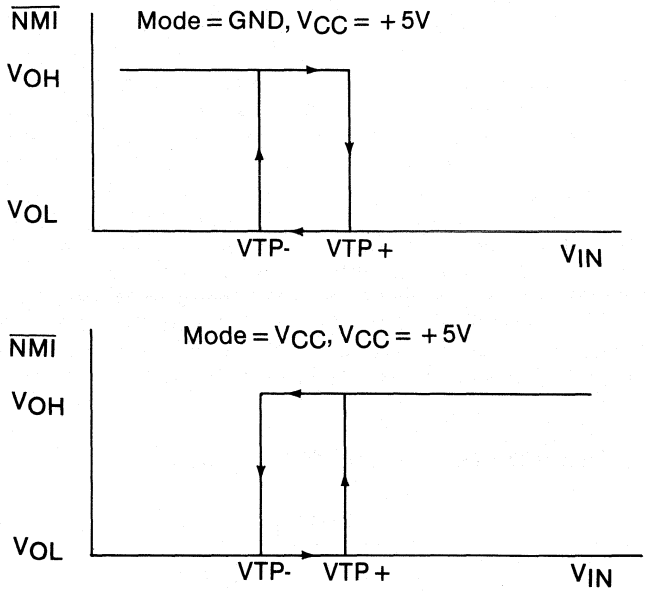
POWER MONITOR BLOCK DIAGRAM Figure 1



POWER UP RESET Figure 2



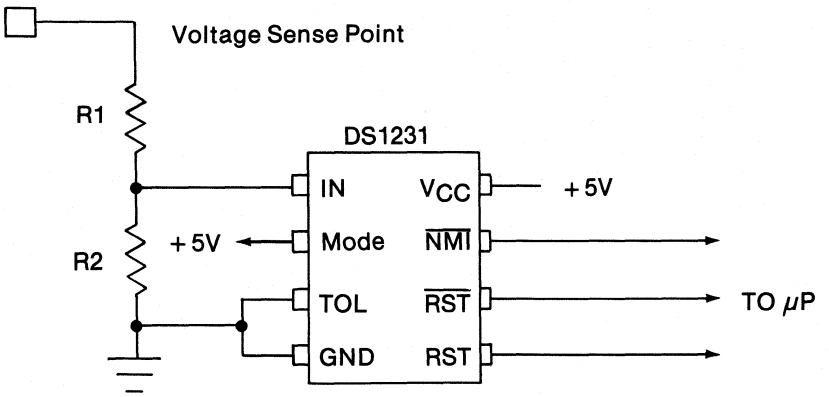
INPUT PIN HYSTERESIS Figure 3



	-20	-35	-50
VTP-	2.3	2.15	2.0
VTP+	2.5	2.5	2.5

NOTE: Hysteresis tolerance is ±60 mV.

APPLICATION WITH MODE PIN CONNECTED TO V_{CC} Figure 4



$$V_{Sense} = \frac{R1 + R2}{R2} \times 2.3 \qquad V_{Max} = \frac{V_{Sense}}{VTP-} \times 5.0$$

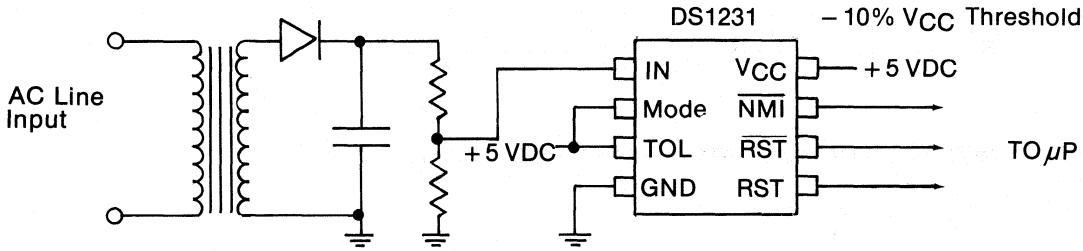
Example: V_{Sense} = 8 volts at Trip Point and a maximum voltage of 17.5V with R2 = 10K

Then $8 = \frac{R1 + 10K}{10K} \times 2.3$ R1 = 25K

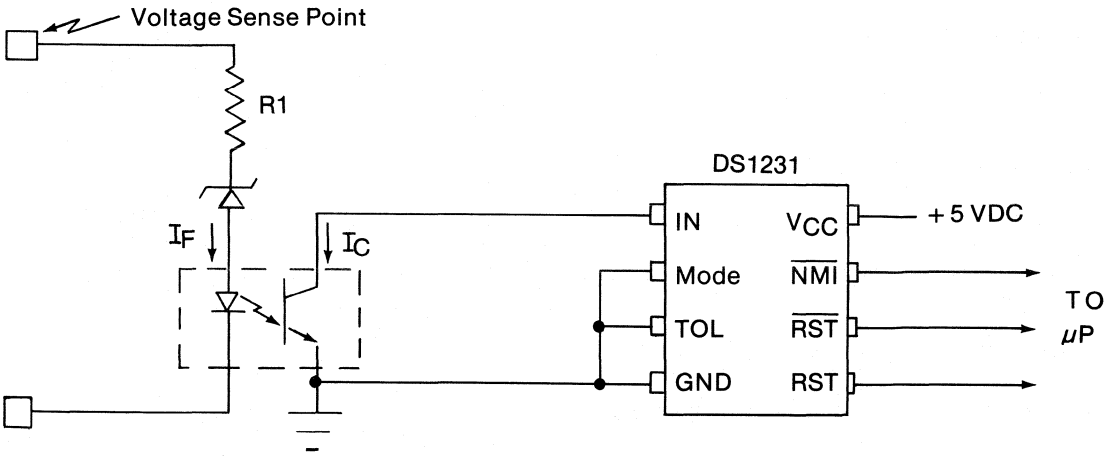
APPLICATION—MODE PIN CONNECTED TO GROUND

When the mode pin is connected to ground, Pin 1 is a current source of 30 uA with a VTP+ of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be sized low enough to allow the opto-isolator to sink the 30 uA of collector current required by Pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5



APPLICATION WITH MODE PIN GROUNDED Figure 6



$$\text{Voltage Sense Point (Trip Value)} = V_Z + \frac{I_C}{CTR} \times R1$$

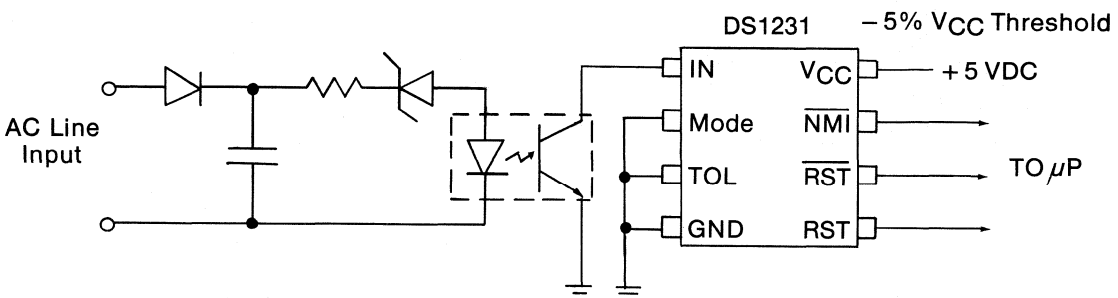
$$CTR = \frac{I_C}{I_F}$$

CTR = Current Transfer Ratio
V_Z = Zener Voltage

Example: CTR = 0.2 $I_C = 30uA$ $I_F = 150uA$
Voltage Sense Point = 105 and $V_Z = 100$ volts

Then $105 = 100 + \frac{30}{0.2} \times R1$ R1 = 33K

AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Pin 1	V_{IN}			V_{CC}	V	1

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1.0		+1.0	uA	2
Output Current @2.4V	I_{OH}	1.0	2.0		mA	
Output Current @0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	3
Input Pin 1 (Mode = GND)	I_C	15	25	50	uA	
Input Pin 1 (Mode = V_{CC})	I_C			0.1	uA	
IN Trip Point (Mode = GND)	VTP	See Figure 3				1
IN Trip Point (Mode = V_{CC})	VTP					1
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

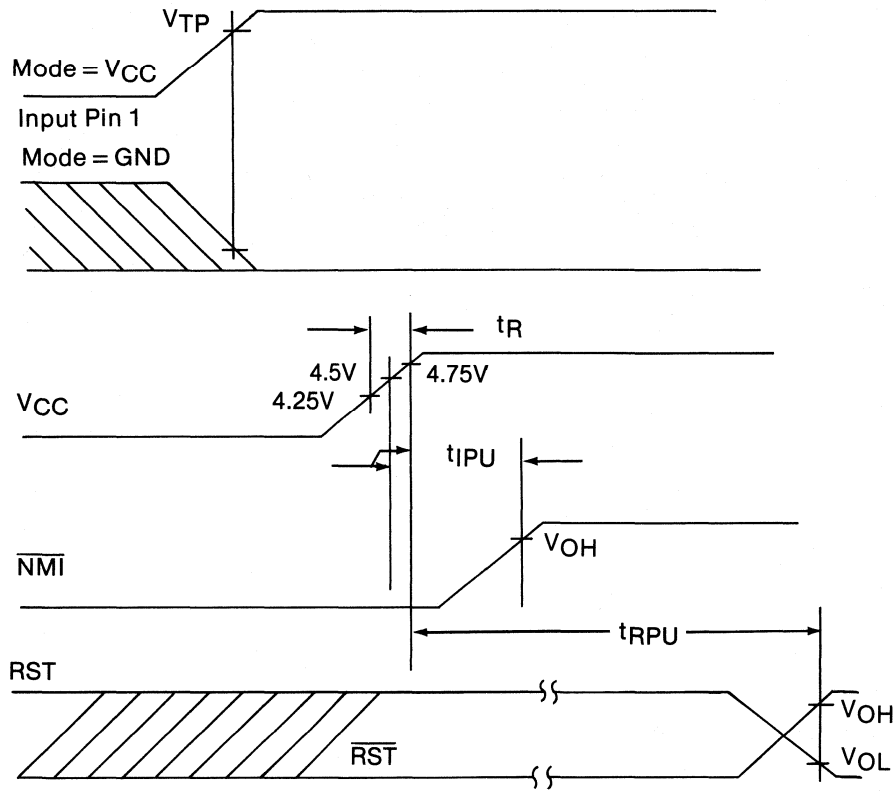
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{TP} to $\overline{NMI}$ Delay	t_{IPD}			1.1	us	
V_{CC} Slew Rate 4.75-4.25V	t_F	300			us	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Detect to $\overline{NMI}$	t_{IPU}			200	us	4
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	250	500	1000	ms	4
V_{CC} Slew Rate 4.25-4.75V	t_R	0			ns	

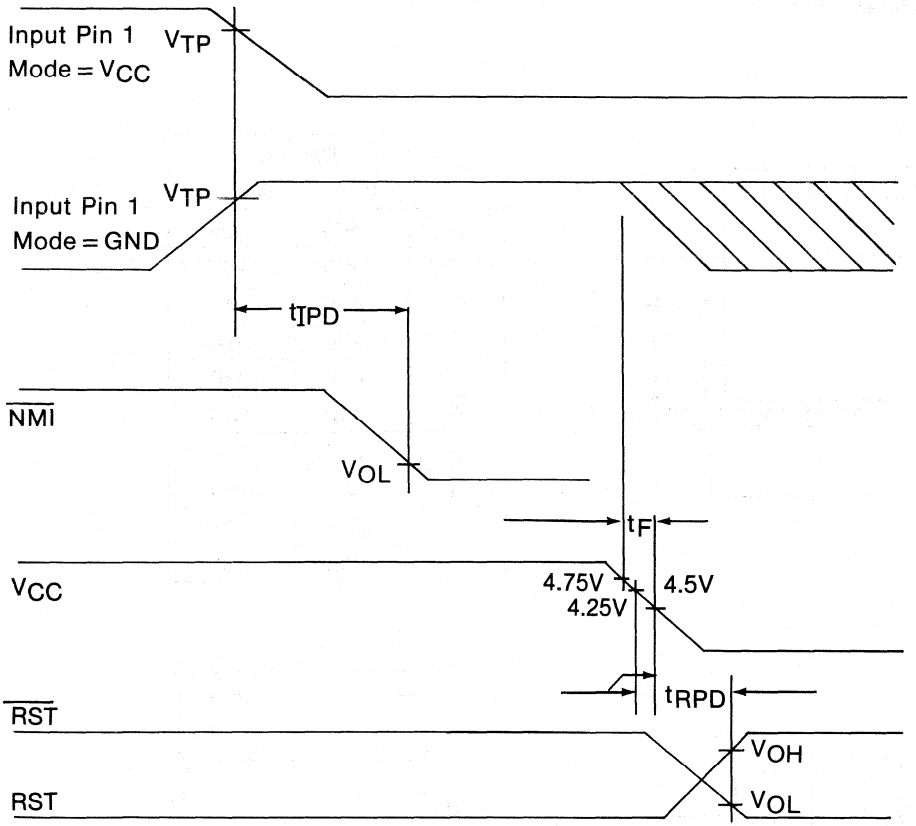
NOTES:

1. All voltages referenced to ground.
2. $V_{CC} = +5.0$ volts with outputs open.
3. Measured with outputs open.
4. $t_R = 5us$.

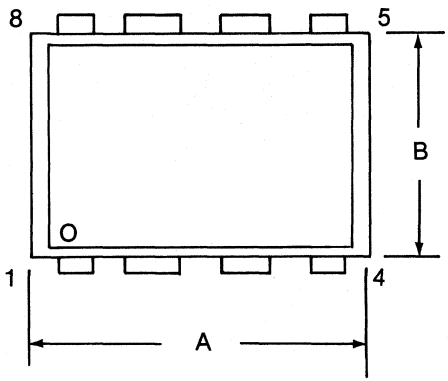
TIMING DIAGRAM—POWER UP



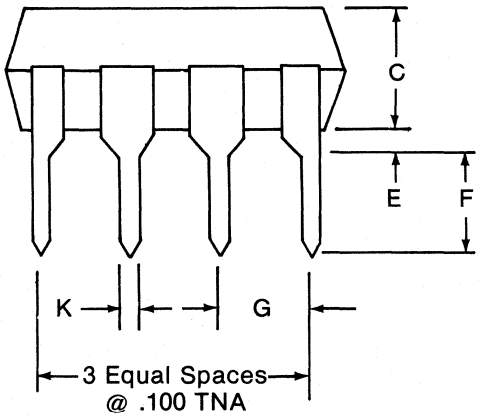
TIMING DIAGRAM—POWER DOWN

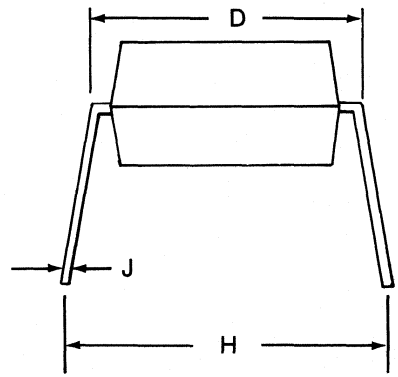


DS1231
Power Monitor



DIM.	INCHES	
	MIN.	MAX.
A	.360	.400
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021





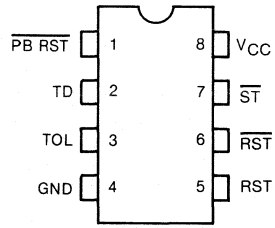
Dallas Semiconductor
Micromonitor

PRELIMINARY
DS1232

FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space saving 8-pin Mini-DIP

PIN CONNECTIONS



PIN NAMES

$\overline{\text{PB RST}}$	- Push Button Reset Input
TD	- Time Delay Set
TOL	- Selects 5% or 10% V_{CC} Detect
GND	- Ground
RST	- Reset Output (Active High)
$\overline{\text{RST}}$	- Reset Output (Active Low, Open Drain)
$\overline{\text{ST}}$	- Strobe Input
V_{CC}	- +5 Volt Power

DESCRIPTION

The DS1232 monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature compensated reference and comparator circuit is used to monitor the status of power (V_{CC}). When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize. The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer which forces the reset signals to the active state if the strobe input is not driven low prior to time out. The watchdog timer function can be set to operate on time-out settings of approximately 100 ms, 500 ms, and 1 second.

OPERATION—POWER MONITOR

The DS1232 provides the function of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC} the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

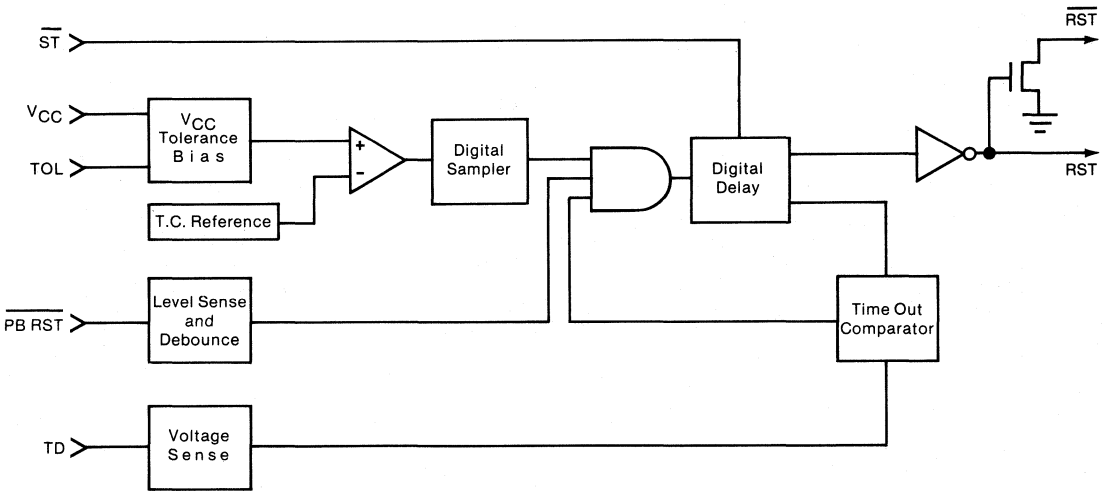
OPERATION—PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

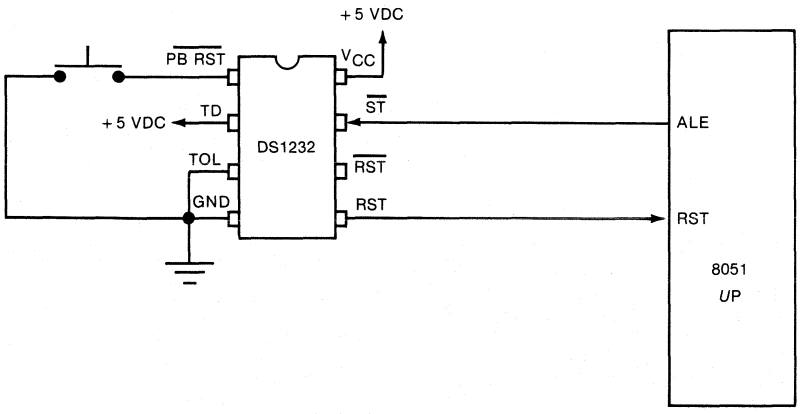
OPERATION—WATCHDOG TIMER

The DS1232 provides a watchdog timer function by forcing RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be 100 ms with TD connected to ground, 500 ms with TD left unconnected, and 1 second with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time out, the watchdog timer is reset and begins to time out again. If the watchdog timer is allowed to time out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time out. A typical example is shown in Figure 3.

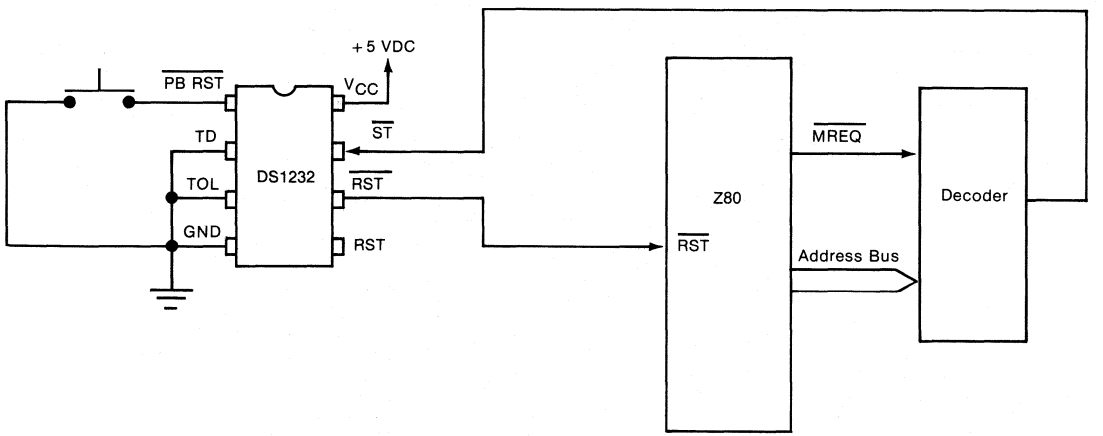
MICROMONITOR BLOCK DIAGRAM Figure 1



PUSHBUTTON RESET Figure 2



WATCHDOG TIMER Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 85°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ Input High Level	V_{IH}	2.0		$V_{CC}+0.3$	V	1
$\overline{ST}$ Input Low Level	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1.0		+1.0	*u*A	2,4
Output Current @2.4V	I_{OH}	−1.0	−2.0		mA	2
Output Current @0.4V	I_{OL}	2.0	3.0		mA	2
Operating Current	I_{CC}		0.5	2.0	mA	3
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

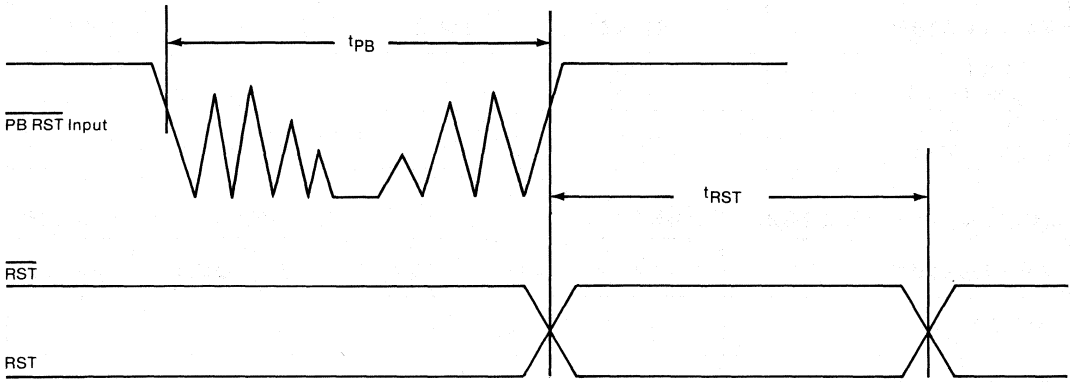
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PB\ RST}$ at Ground	t_{PB}	10			ms	
RESET Active Time	t_{RST}	250	410	500	ms	
$\overline{ST}$ Pulse Width	t_{ST}	10			ns	
V_{CC} Detect to $\overline{RST}$ and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate 4.75V - 4.25V	t_F	300			ns	
V_{CC} Detect to $\overline{RST}$ and $\overline{RST}$	t_{RPV}	250	410	500	ms	5
V_{CC} Slew Rate 4.25V - 4.75V	t_R	0			ns	

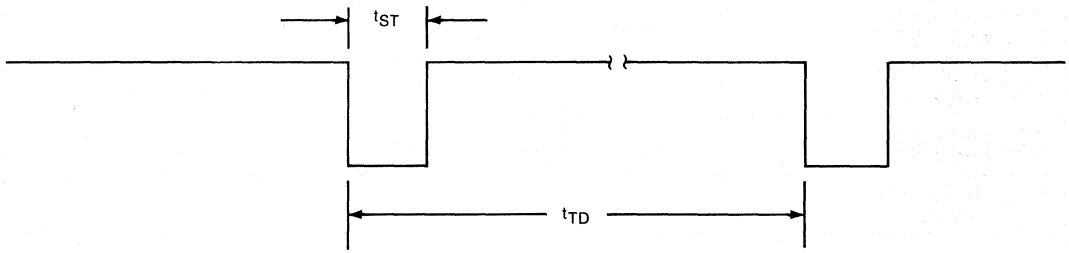
NOTES:

1. All voltages referenced to ground.
2. $V_{CC} = +5.0$ volts with outputs open.
3. Measured with outputs open.
4. $\overline{PB\ RST}$ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
5. $t_R = 5$ *u*s.

TIMING DIAGRAM—PUSHBUTTON RESET



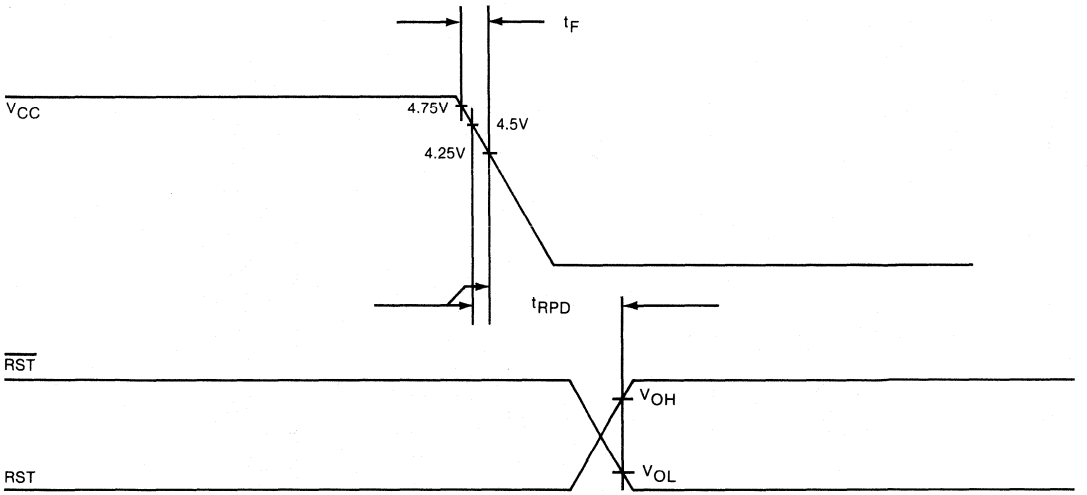
TIMING DIAGRAM—STROBE INPUT



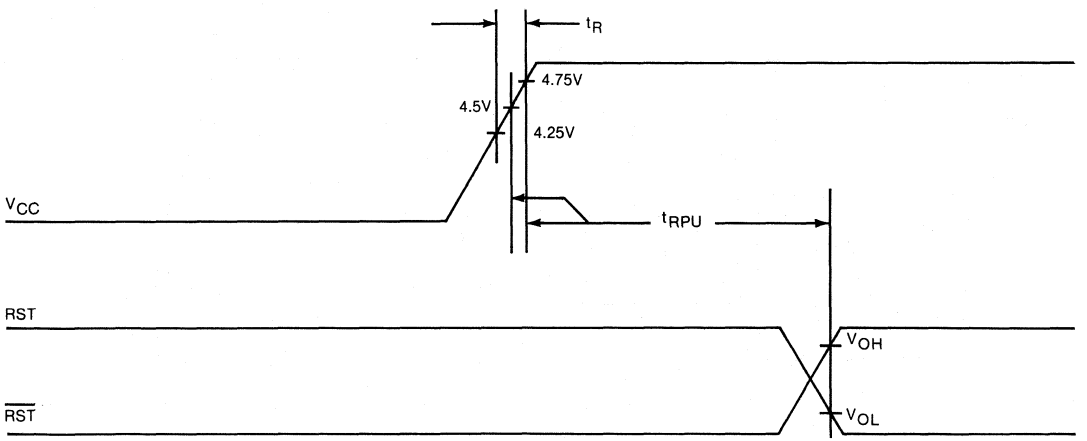
t_{TD} = 100 ms maximum with TD pin at Ground
t_{TD} = 500 ms maximum with TD pin floating
t_{TD} = 1 sec maximum with TD pin connected to V_{CC}

NOTE:
t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}. t_{TD} times are given as maximum. The minimum time is 50% of maximum.

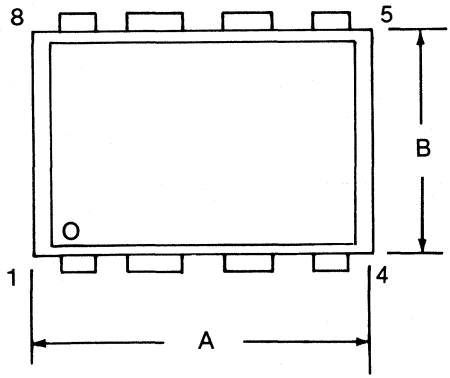
TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP



DS1232
Micromonitor



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C	.120	.140
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F	.110	.130
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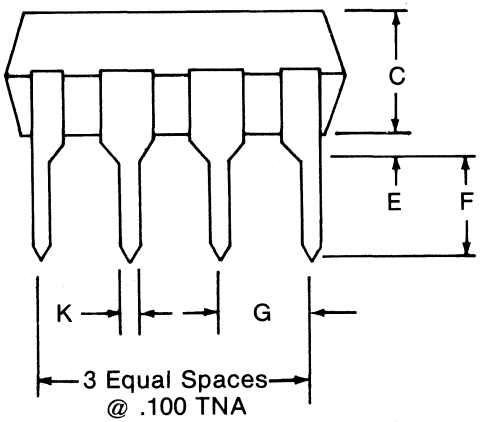
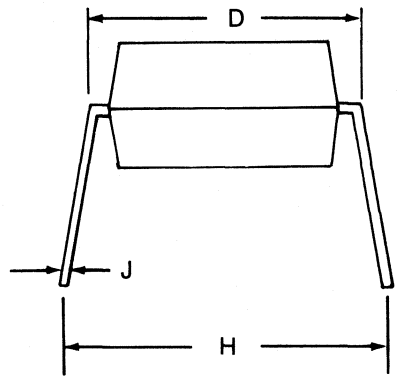
J	.008	.012
K	.015	.021



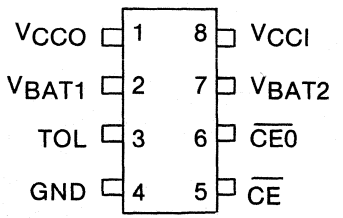


Dallas Semiconductor
Nonvolatile Controller — *DS1210*

FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8 pin mini-DIP
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the V_{CC} Switch

PIN CONNECTIONS



PIN NAMES

1 - V_{CCO} - +5 V Outgoing
2 - V_{BAT1} - + Battery 1
3 - TOL - Power Supply Tolerance
4 - GND - Ground
5 - $\overline{CE}$ - Chip Enable Input
6 - $\overline{CEO}$ - Chip Enable Output
7 - V_{BAT2} - + Battery 2
8 - V_{CCI} - +5 V Incoming

DESCRIPTION

The DS1210 is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8 pin mini-DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 nonvolatile controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

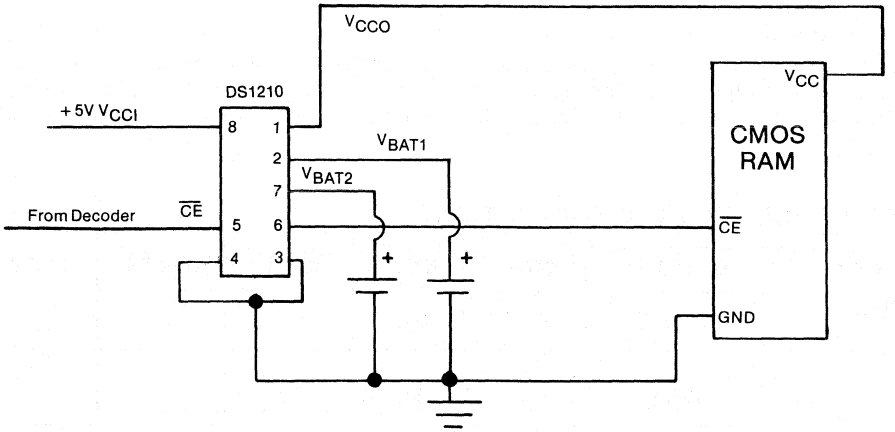
OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CC1}) depending on which is greater. This switch has a voltage drop of less than 0.2V.The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable ($\overline{CEO}$). The third function of write protection is accomplished by holding the $\overline{CEO}$ output signal to within 0.2 volts of the V_{CCI} or battery supply. If $\overline{CE}$ input is low at the time power fail detection occurs, the CEO output is kept in its present state until $\overline{CE}$ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CE}$ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. In applications where battery reliability is not a concern only one battery need be connected to B_{AT1} or B_{AT2} pin, with the other battery pin grounded.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.5 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power up to prevent spurious writes.

FIGURE 1

SECTION A — BATTERY BACKUP

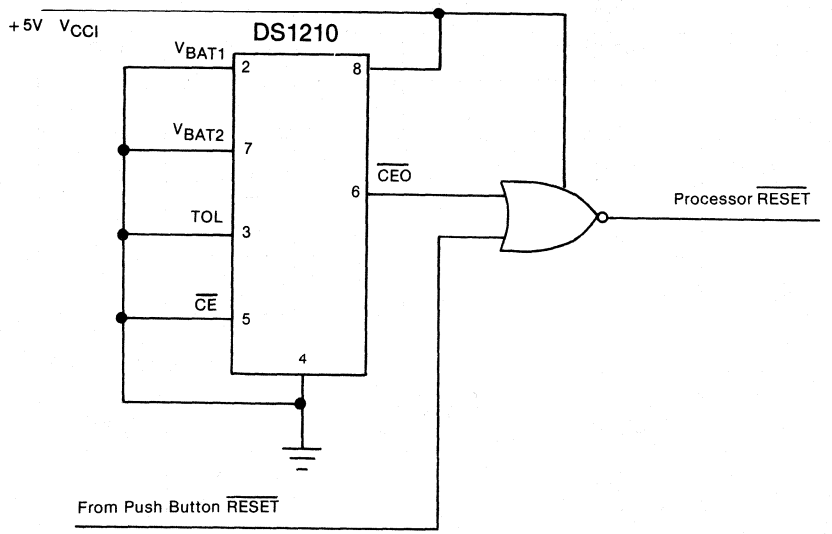


BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I_{BAT}	- 100 nA
RAM I_{CC02}	- 10 uA
Total Drain	- 10.1*u*A

SECTION B — PROCESSOR RESET



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to 85°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
PIN 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1,2

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C , V_{CCI} = 4.75V to 5.5V, PIN 3 = GND) (V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

Supply Current	I_{CCI}			15	mA	3
Supply Voltage	V_{CCO}	V_{CC} − 0.2			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
$\overline{CE0}$ Output @2.4V	I_{OH}	−1.0			mA	5
$\overline{CE0}$ Output @ 0.4V	I_{OL}			4.0	mA	5

(0°C to 70°C, $V_{CCI} < V_{BAT}$)

$\overline{CE0}$ Output	V_{OHL}	V_{CC} − 0.2 V_{BAT} − 0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2,3
Battery Backup Curent @$V_{CCO} = V_{BAT}$ − 0.3V	I_{CC02}			50	uA	6,7

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS

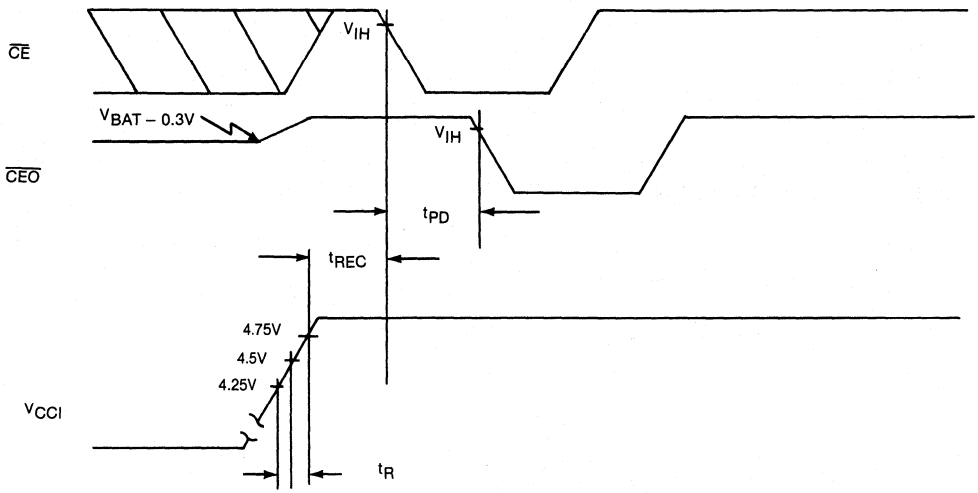
(0°C - 70°C, V_{CCI} = 4.75 - 5.5V, PIN 3 = GND)
(V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

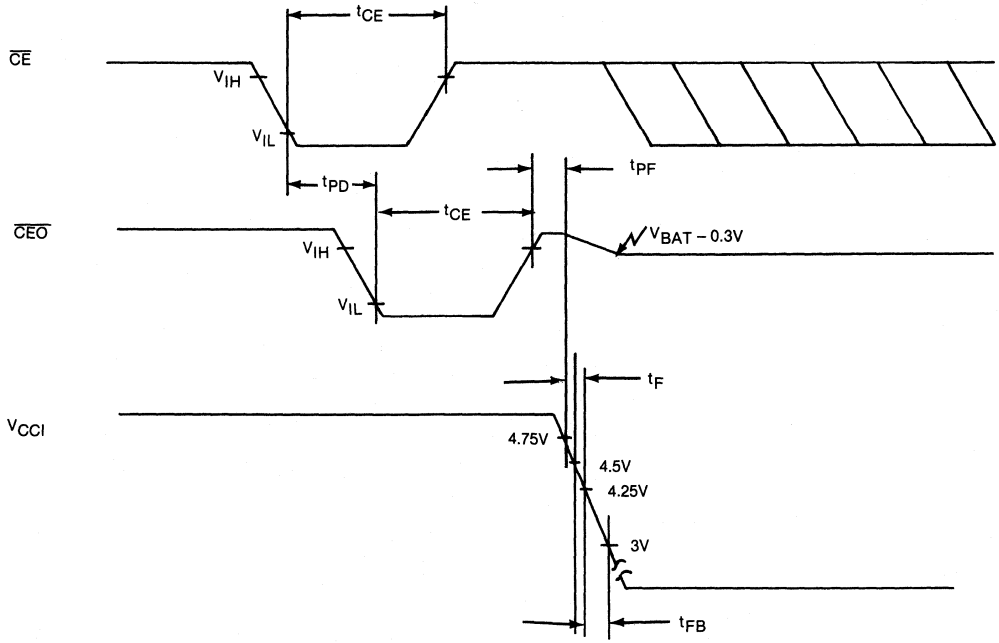
(0°C to 70°C, V_{CCI} < 4.75V, PIN 3 = GND)
(V_{CCI} < 4.5V, PIN 3 = V_{CCO})

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			us	
V_{CC} Slew Rate Power Down	t_{FB}	10			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	us	7,8

TIMING DIAGRAM — POWER UP

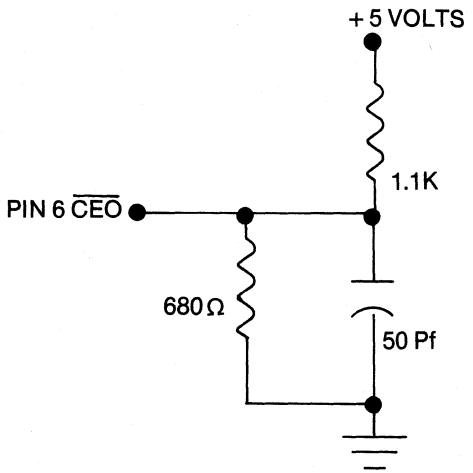


TIMING DIAGRAM — POWER DOWN



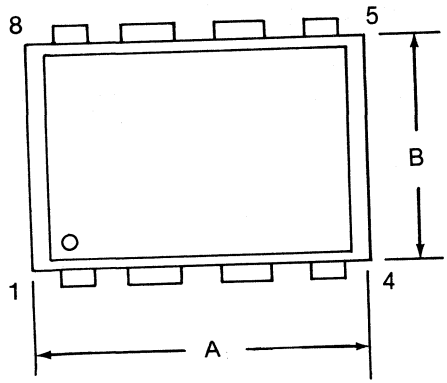
NOTES:

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and $\overline{CE0}$ open.
4. I_{CC01} is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. I_{CC02} is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
7. t_{CE} max must be met to insure data integrity on power loss.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery backup mode.



OUTPUT LOAD
Figure 2

DS1210
Nonvolatile Controller



DIM.	INCHES	
	MIN.	MAX.
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G	.090	.110
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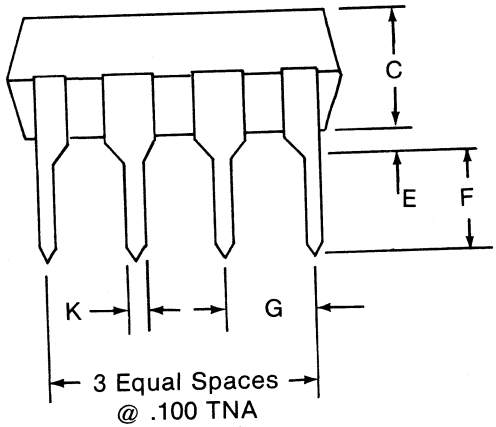
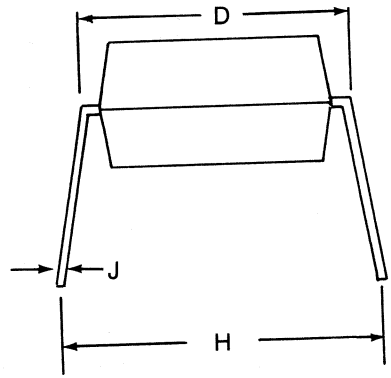
J	.008	.012
K	.015	.021



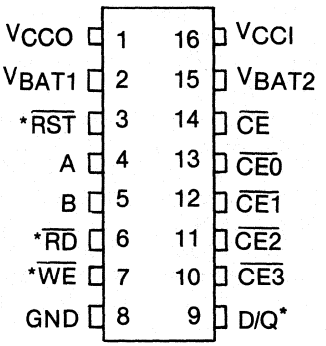


Dallas Semiconductor
Nonvolatile Controller/Decoder — *DS1221*

FEATURES

- Converts CMOS RAMs into Nonvolatile Memories
- Data is automatically protected during power loss
- 2 to 4 Decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power up
- Full ±10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-Pin 0.3-inch DIP saves P.C. board space.

PIN CONNECTIONS



PIN NAMES

*A, B	- Address Inputs
CE	- Chip Enable Input
CE0-CE3	- Chip Enable Outputs
VBAT1	- + Battery 1
VBAT2	- + Battery 2
*RST	- Reset
VCCI	- + 5V Incoming
VCCO	- + 5V Outgoing
*RD	- Read Input
*WE	- Write Input
*D/Q	- Data Input/Output

*Used with optional security circuit only and must be connected to ground in all other cases

DESCRIPTION

The DS1221 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unauthorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, ten years of nonvolatile operation can be achieved.

CONTROLLER/DECODER OPERATION

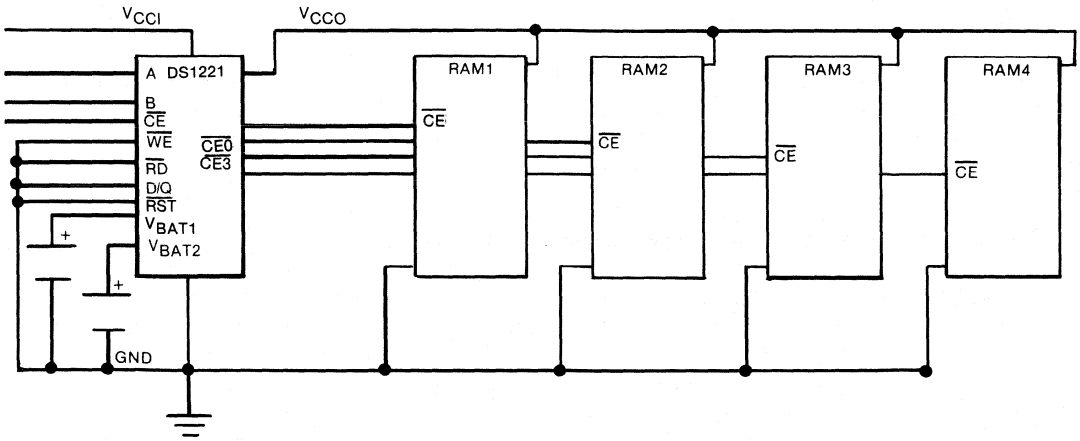
The DS1221 nonvolatile controller/decoder performs six circuit functions required to decode and battery back up a bank of up to four CMOS RAMs. First, a 2 to 4 decoder provides selection of one of four RAMs (See Figure 1). Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater, to the V_{CCO} pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller/decoder provides is power fail detection. The DS1221 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables ($\overline{CE0}$ through $\overline{CE3}$). The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE3}$) to within 0.2 volts of V_{CCI} or battery supply. If the Chip Enable Input ($\overline{CE}$) is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2 to 4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data loss. Each time that V_{CCI} power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller/decoder provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

NONVOLATILE CONTROLLER/DECODER Figure 1

	INPUTS			OUTPUTS			
V_{CCI}	$\overline{CE}$	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
≥ 4.5	H	X	X	H	H	H	H
< 4.25	X	X	X	H	H	H	H
≥ 4.5	L	L	L	L	H	H	H
≥ 4.5	L	L	H	H	L	H	H
≥ 4.5	L	H	L	H	H	L	H
≥ 4.5	L	H	H	H	H	H	L

H = High Level
L = Low Level
X = Irrelevant

TYPICAL APPLICATION Figure 2



Battery Backup Current Drain

DS1221	- .1 uA @ 25° C
RAM-5564 × 4	- .8 uA @ 25° C
Total	.9 uA @ 25° C

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to 85°C
Soldering Temperature 260°C for 10 Sec
Short Circuit Output Current 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1,2

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

Supply Current	I_{CCI}			15	mA	3
Supply Voltage	V_{CCO}	$V_{CC}-0.2$			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	−1.0		+1.0	μA	
Output Leakage	I_{LO}	−1.0		+1.0	μA	
$\overline{CEO}$-$\overline{CE3}$, DQ Output @2.4V	I_{OH}	−1.0			mA	5
$\overline{CEO}$-$\overline{CE3}$, DQ Output @ 0.4V	I_{OL}			4.0	mA	5

(0°C to 70°C V_{CC} <4.25)

$\overline{CEO}$-$\overline{CE3}$ Output	V_{OHL}	$V_{CC}-0.2$ $V_{BAT}-0.2$			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.1	μA	3
Battery Backup Current	I_{CCO2}			40	μA	6,7

CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

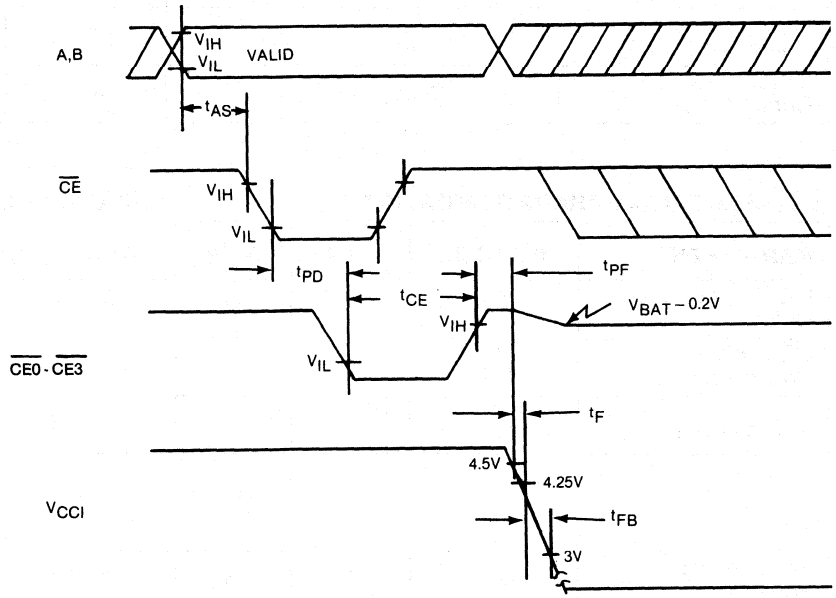
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Set Up	t_{AS}	20			ns	

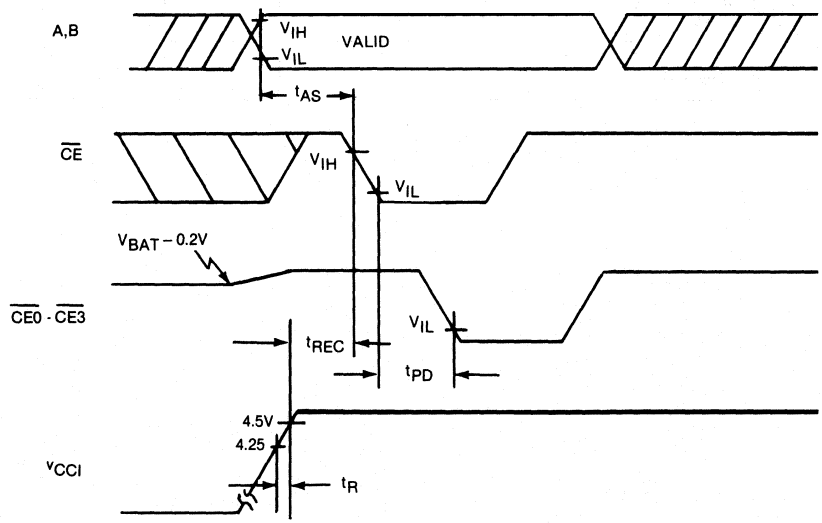
(0 °C to 70 °C, V_{CC} 4.5V)

Recovery at Power Up	t_{REC}	2	5	10	ms	
V_{CC} Slew Rate 4.5 - 4.25V	t_F	300			us	
V_{CC} Slew Rate 4.25 - 3V	t_{FB}	10			us	
V_{CC} Slew Rate 4.25 - 4.5V	t_R	0			us	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	us	7,8

TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP

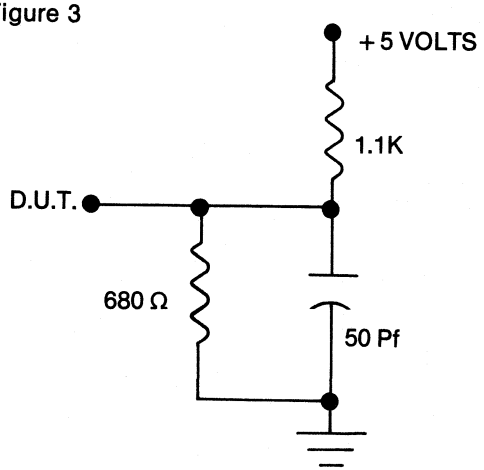


NOTES:

1. All voltages are referenced to ground
2. Only one battery input is required
3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE3}$ open
4. I_{CCO1} is the maximum average load which the DS1221 can supply to the memories
5. Measured with a load as shown in Figure 3
6. I_{CCO2} is the maximum average load current which the DS1221 can supply to the memories in the battery backup mode
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE3}$ can only sustain leakage current in the battery backup mode
8. t_{CE} max must be met to insure data integrity on power loss

OUTPUT LOAD

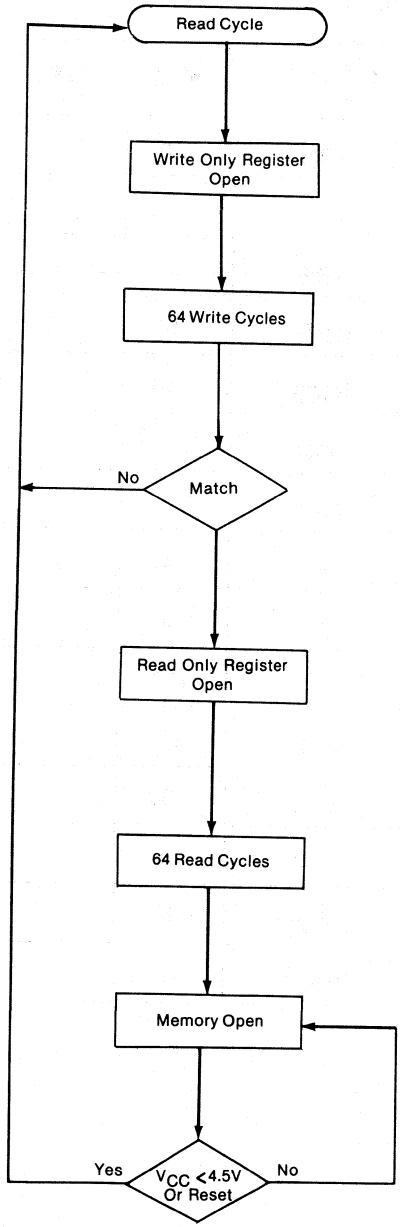
Figure 3



SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 1). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the cartridge without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register may be used by software to determine if the cartridge will be permitted to be used with that particular system. After the 64th read cycle has been executed the cartridge is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V_{CC} falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.
Note: Contact Dallas Semiconductor sales office for code assignment.

SECURITY SEQUENCE
Figure 1



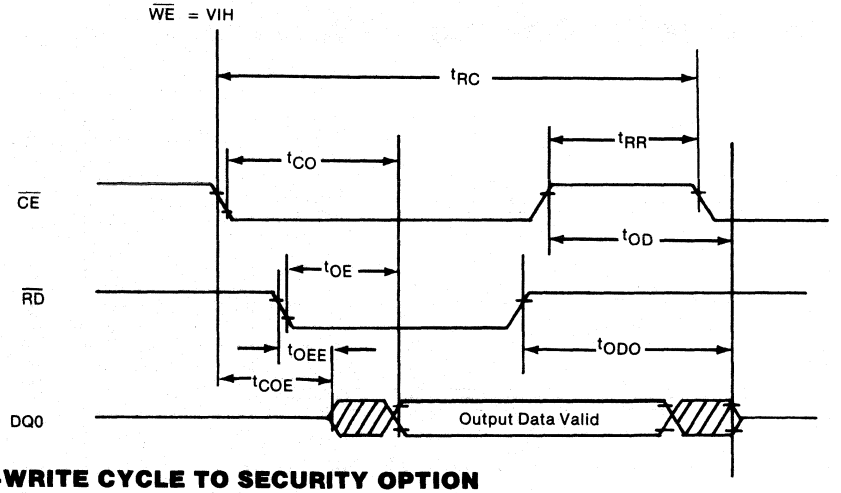
SECURITY OPTION

A.C. ELECTRICAL CHARACTERISTICS

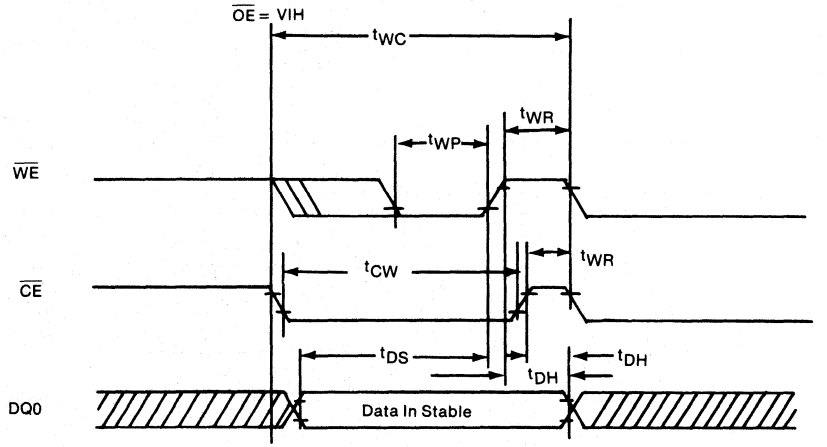
(0 °C - 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Read Cycle Time	t_{RC}	250			ns
$\overline{CE}$ Access Time	t_{CO}			200	ns
$\overline{RD}$ Access Time	t_{OE}			100	ns
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns
$\overline{RD}$ To Output Low Z	t_{OEE}	10			ns
$\overline{CE}$ To Output High Z	t_{OD}			100	ns
$\overline{RD}$ To Output High Z	t_{ODO}			100	ns
Read Recovery	t_{RR}	50			ns
Write Cycle	t_{WC}	250			ns
Write Pulse Width	t_{WP}	170			ns
Write Recovery	t_{WR}	50			ns
Data Set Up	t_{DS}	100			ns
Data Hold Time	t_{DH}	0			ns
$\overline{CE}$ Pulse Width	t_{CW}	170			ns
Reset Pulse Width	t_{RST}	200			ns

TIMING DIAGRAM—READ CYCLE TO SECURITY OPTION



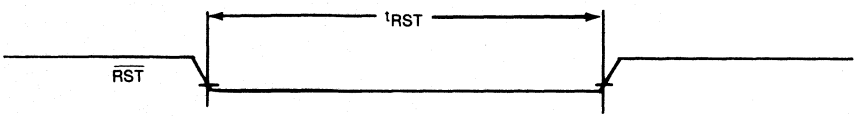
TIMING DIAGRAM—WRITE CYCLE TO SECURITY OPTION



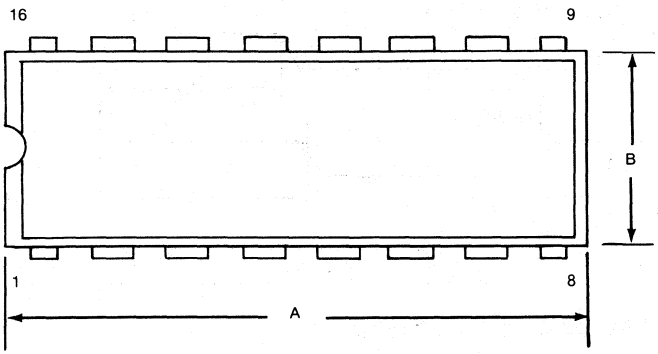
NOTES:

1. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

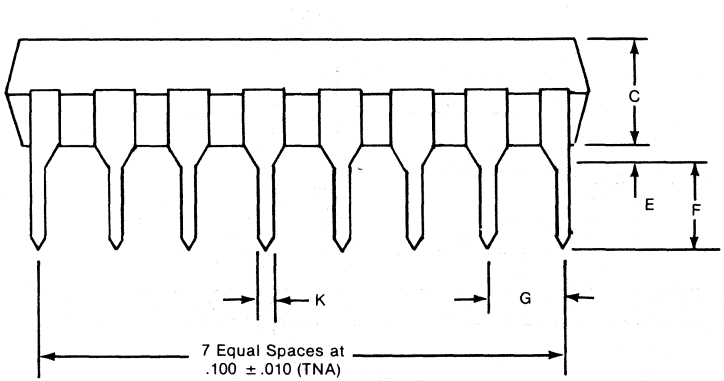
TIMING DIAGRAM—RESET FOR SECURITY OPTION

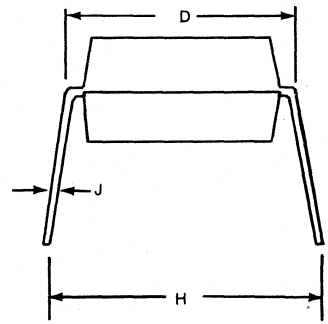


DS1221
Nonvolatile Controller/Decoder



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021



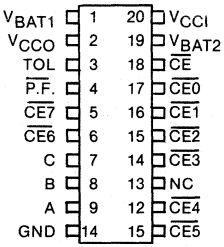


Dallas Semiconductor
Nonvolatile Controller/Decoder **DS1211**

FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 3 to 8 decoder provides control for up to 8 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection

PIN CONNECTIONS



PIN NAMES

A, B, C	- Address Inputs
$\overline{CE}$	- Chip Enable Input
$\overline{CE0}$-$\overline{CE7}$	- Chip Enable Outputs
GND	- Ground
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
TOL	- Power Supply Tolerance
V_{CCI}	- +5V Incoming
V_{CCO}	- +5V Outgoing
$\overline{P.F.}$	- Power Fail
N.C.	- No Connection

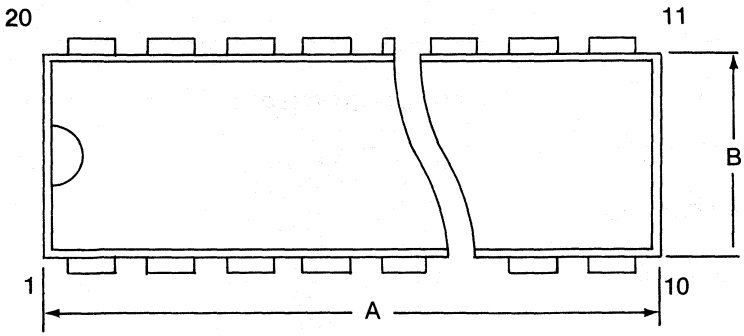
DESCRIPTION

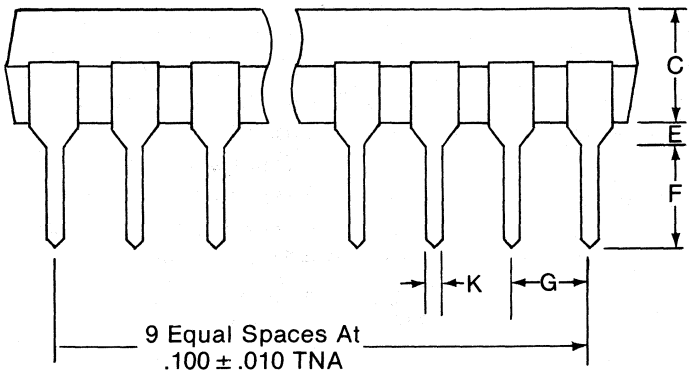
The DS1211 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1211 nonvolatile controller/decoder chip and lithium batteries, ten years of nonvolatile RAM operation can be achieved for up to eight CMOS memories.

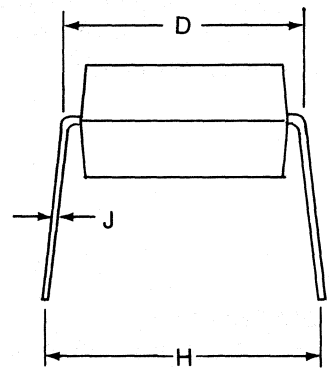
See the data sheet for the DS1212 for electrical specifications and operation.

DS1211
Nonvolatile Controller





DIM.	INCHES	
	MIN.	MAX.
A	.960	1.040
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021

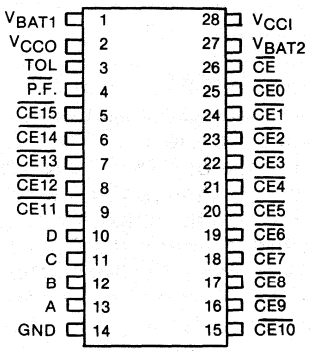


Dallas Semiconductor
Nonvolatile Controller/Decoder — *DS1212*

FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection

PIN CONNECTIONS



PIN NAMES

A, B, C, D	- Address Inputs
$\overline{CE}$	- Chip Enable
$\overline{CE0}$-$\overline{CE15}$	- Chip Enable Outputs
GND	- Ground
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
TOL	- Power Supply Tolerance
V_{CCI}	- +5V Incoming
V_{CCO}	- +5V Outgoing
$\overline{P.F.}$	- Power Fail

DESCRIPTION

The DS1212 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 nonvolatile controller/decoder chip and lithium batteries, ten years of nonvolatile RAM operation can be achieved for up to sixteen CMOS memories.

OPERATION

The DS1212 nonvolatile controller/decoder performs six circuit functions required to decode and battery back up a bank of sixteen RAMs. First, the 4 to 16 decoder provides selection of one of sixteen RAMs. Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller/decoder provides is power fail detection. The DS1212 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.75 volts, or 4.5 volts depending on the level of the tolerance Pin 3, a precision comparator outputs a power fail detect signal to the decoder/chip enable logic and the $\overline{PF}$ signal is driven low. The $\overline{PF}$ signal will remain low until V_{CCI} is back in normal limits. The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE15}$) to within 0.2 volts of V_{CCI} or battery supply. If $\overline{CE}$ is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4 to 16 decoder, shown in Figure 1. The fifth function the DS1212 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted. The sixth function of the nonvolatile controller/decoder provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

NONVOLATILE CONTROLLER/DECODER Figure 1

INPUTS						OUTPUTS															
V_{CCI}	CE	D	C	B	A	CE0	CE1	CE2	CE3	CE4	CE5	CE6	CE7	CE8	CE9	CE10	CE11	CE12	CE13	CE14	CE15	PF
≥ 4.75	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
< 4.75	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
≥ 4.75	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
≥ 4.75	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
≥ 4.75	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
≥ 4.75	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
≥ 4.75	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
≥ 4.75	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
≥ 4.75	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
≥ 4.75	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
≥ 4.75	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = High Level
L = Low Level
X = Irrelevant

NOTE:
V_{CCI} input is 250 mV lower when TOL PIN 3 = V_{CCO}

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to 85°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
PIN 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1,2

D.C. ELECTRICAL CHARACTERISTICS
(0°C to 70°C, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)
(0°C to 70°C, V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			15	mA	3
Supply Current @V_{CCO} = V_{CCI} − 0.2	I_{CCO1}			80	mA	1,4
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
$\overline{CE0}$-$\overline{CE15}$ Output @2.4V	I_{OH}	−1.0			mA	5
$\overline{CE0}$-$\overline{CE15}$ Output @ 0.4V	I_{OL}			4.0	mA	5

(0°C to 70°C, V_{CCI} < V_{BAT})

$\overline{CE0}$-$\overline{CE15}$ Output	V_{OHL}	V_{BAT} − 0.2			V	3,7
Battery Current	I_{BAT}			0.1	uA	2,3
Battery Backup Current @V_{CCO} = V_{BATI} − 0.5V	I_{CC02}			100	uA	6

CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS

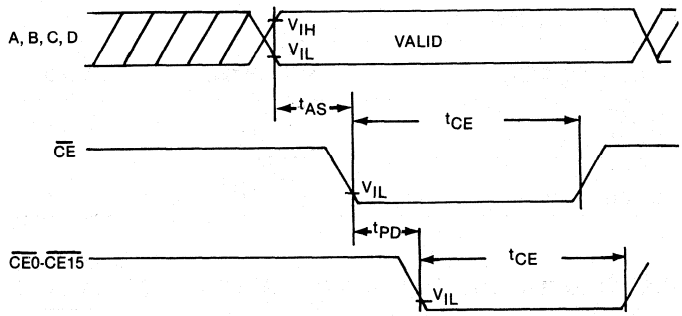
(0°C to 70°C, V_{CCI} = 4.75 to 5.5V, Pin 3 = GND)
(0°C to 70°C , V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	13	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Set Up	t_{AS}	20			ns	

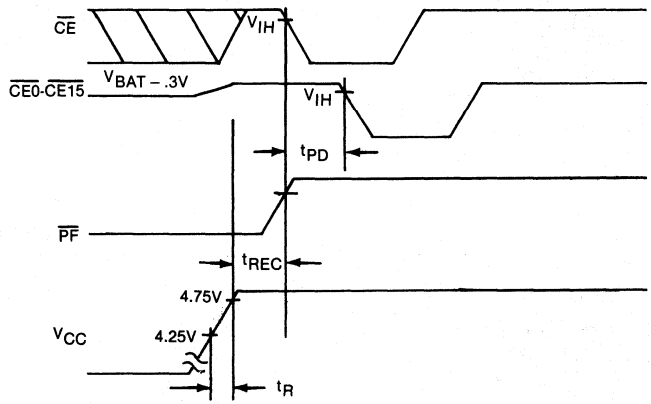
(0°C to 70°C, V_{CCI} < 4.75V, Pin 3 = GND)
(0°C to 70°C, V_{CCI}< 4.5V, Pin 3 = V_{CCO})

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			us	
V_{CC} Slew Rate Power Down	t_{FB}	10			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	us	7,8
Power Fail to $\overline{PF}$ Low	t_{PFL}	300			us	

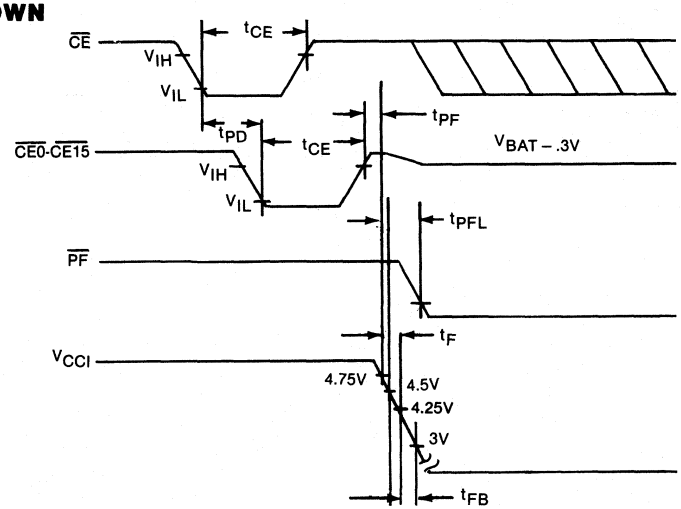
TIMING DIAGRAM—DECODER



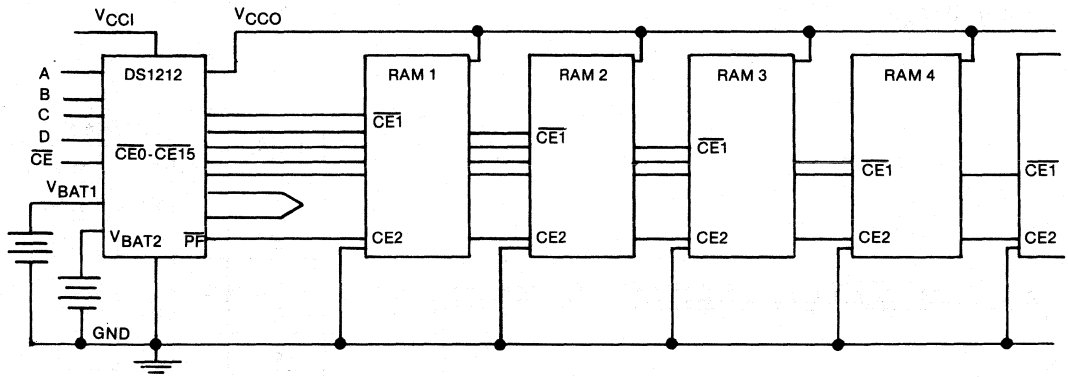
TIMING DIAGRAM—POWER UP



TIMING DIAGRAM—POWER DOWN



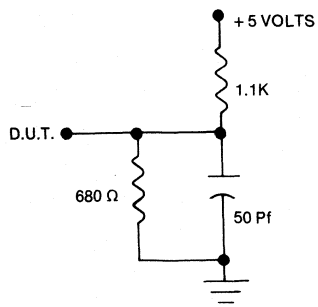
TYPICAL APPLICATION Figure 2

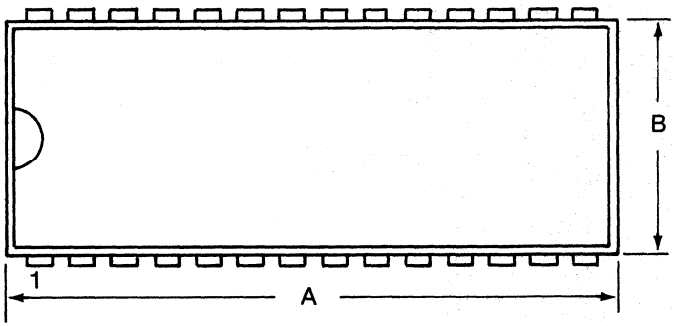


NOTES:

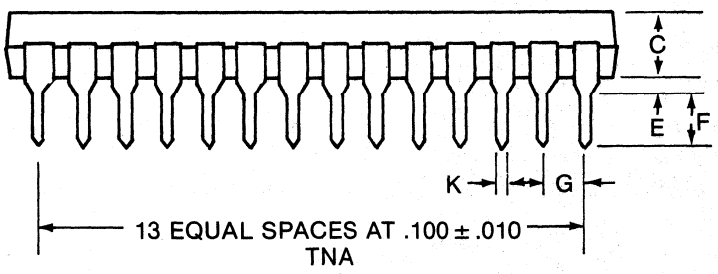
1. All voltages are referenced to ground
2. Only one battery input is required
3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE15}$ open
4. I_{CC01} is the maximum average load which the DS1212 can supply to the memories
5. Measured with a load as shown in Figure 3
6. I_{CC02} is the maximum average load current which the DS1212 can supply to the memories in the battery backup mode.
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE15}$ can only sustain leakage current in the battery backup mode
8. t_{CE} max must be met to insure data integrity on power loss

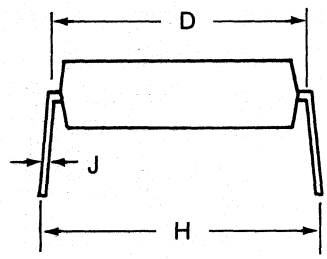
OUTPUT LOAD Figure 3



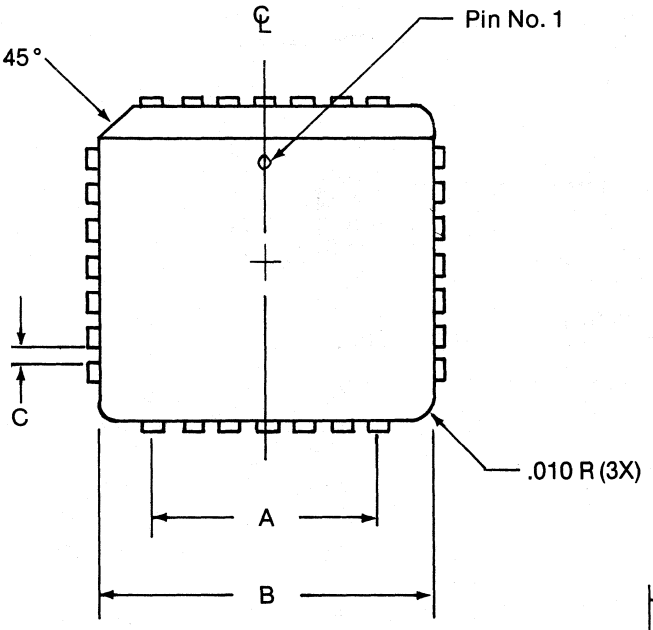


DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

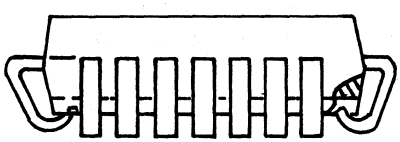


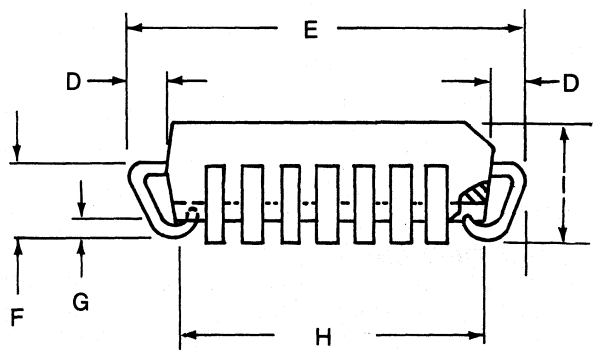


DS 1212Q



DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.167	.173





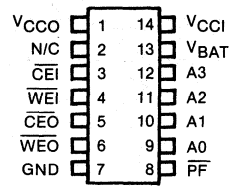
Dallas Semiconductor
Conditional Nonvolatile Controller

PRELIMINARY
DS1234

FEATURES

- Converts CMOS static RAMs into nonvolatile memories
- Software controlled write inhibit
- Software controlled battery disconnect extends battery life
- Unconditionally write protects when V_{CC} is out of tolerance
- Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the V_{CC} switch

PIN CONNECTIONS



PIN NAMES

Pin 1	- V_{CCO}	RAM Supply
Pin 2	- N/C	No Connection
Pin 3	- $\overline{CEI}$	Chip Enable Input
Pin 4	- $\overline{WEI}$	Write Enable Input
Pin 5	- $\overline{CEO}$	Chip Enable to RAM
Pin 6	- $\overline{WEO}$	Write Enable to RAM
Pin 7	- GND	Ground
Pin 8	- $\overline{PF}$	Power Fail Output
Pins 9-12	- A0-A3	Address Inputs
Pin 13	- V_{BAT}	Battery Input
Pin 14	- V_{CCI}	+5V Supply

DESCRIPTION

The DS1234 is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory with the added features of two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, Chip Enable and Write Enable to the RAM are inhibited to accomplish write protection and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write enable to the RAM and the battery back-up circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery back-up is not needed.

OPERATION

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery back-up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}), depending on whichever is greater. This switch has a voltage drop of less than 0.2V. The second function which the nonvolatile controller provides is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out of tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage, V_{TP}, at which power fail is detected is defined as 1.26 times V_{BAT}. The third function of write protection is accomplished by holding the $\overline{CEO}$ and $\overline{WEO}$ output signals to within 0.2 volts of the V_{CCI} or battery supply. In addition to the nonvolatile controller functions, the DS1234 supplies two software selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence which will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer to clock zero. Each four-bit compare word is clocked into the DS1234 on the low-going edge of $\overline{CEI}$. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven, and the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch which inhibits the write enable to the RAM ($\overline{WEO}$). A logic one in this location allows read/write operations so that $\overline{WEO}$ will follow $\overline{WEI}$ and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 through 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010, respectively, activates the nonvolatile controller and data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation. At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 through 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial V_{CC} power the write enable will be set in read/write operation ($\overline{WEI} = \overline{WEO}$).

ADDRESS INPUT PATTERN Table 1

	Cycle Number															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_3	1	0	1	0	0	0	1	1	0	1	0	*	*	*	*	*
A_2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

*See Table 2

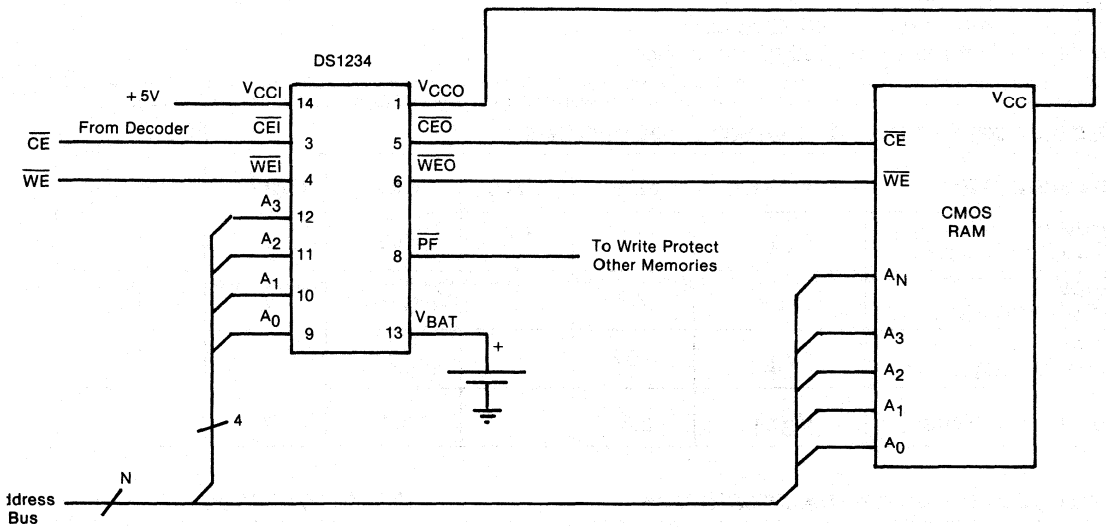
CONTROL SELECT Table 2

$\overline{WE}$	Battery Control				Operation
11	**12**	**13**	**14**	**15**	
0	×	×	×	×	Read Only Operation
1	×	×	×	×	Read/Write Operation
×	1	0	1	0	Enables Nonvolatile Controller*

× Don't Care

*Any other combination turns controller off

Figure 1


DS1234
+5V
From Decoder
$\overline{CE}$
$\overline{WE}$
V_{CCI}
$\overline{CEI}$
$\overline{WEI}$
A_3
A_2
A_1
A_0
14
3
4
12
11
10
9
1
5
6
8
13
V_{CCO}
$\overline{CEO}$
$\overline{WEO}$
$\overline{PF}$
V_{BAT}
+
To Write Protect
Other Memories
4
N
Address
Bus
V_{CC}
$\overline{CE}$
$\overline{WE}$
CMOS
RAM
A_N
A_3
A_2
A_1
A_0

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to 85°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Power Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Input Low Voltage	V_{IL}	−0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	2
Supply Current @ $V_{CCO}=V_{CCI}-0.2$	I_{CCO}			80	mA	3
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	4
Output Current @ 0.4V	I_{OL}			4.0	mA	4

(0°C to 70°C $V_{CCI}<V_{BAT}$)

$\overline{CEO}$, $\overline{WEO}$ Output	V_{OHL}	$V_{BAT}-0.2$			V	6
Battery Current	I_{BAT}			0.1	uA	7
Battery Backup Current @$V_{CCO}=V_{BAT}-0.3V$	I_{CC0}			100	uA	5

CAPACITANCE ($t_A = 25\,°C$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

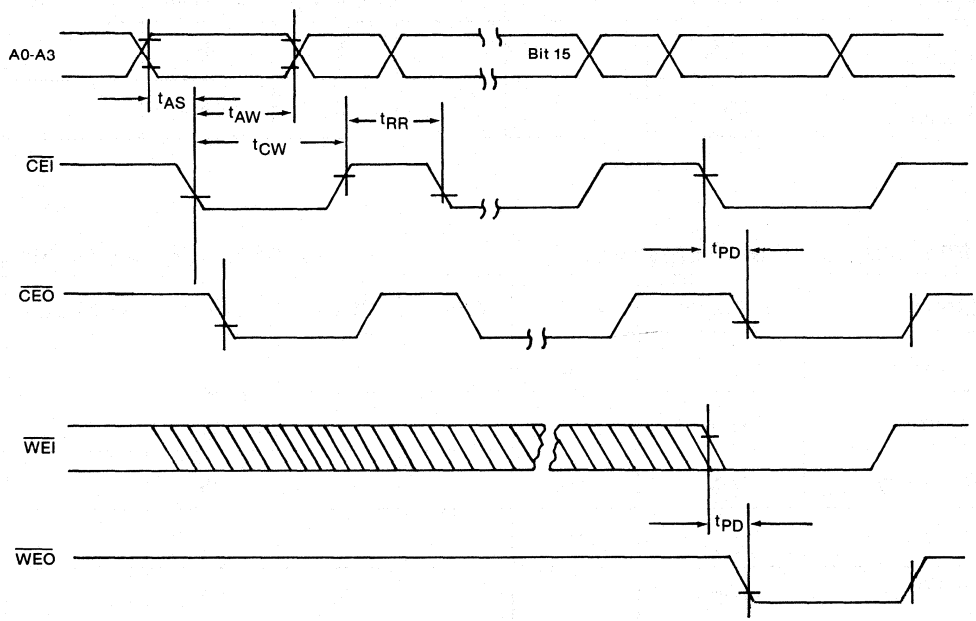
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
$\overline{CEI}$ Pulse Width	t_{CW}	110			ns	
Propagation Delay	t_{PD}			20	ns	

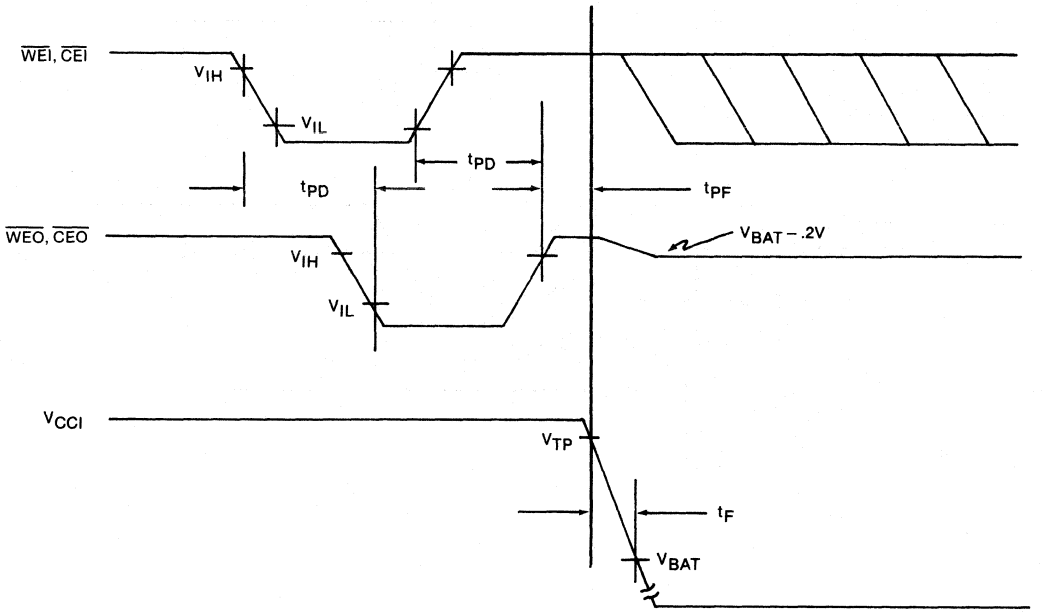
(0 °C to 70 °C, $V_{CCI} < V_{TP}$)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate Power Down	t_F	0			*us*	
V_{CC} Slew Rate Power Up	t_R	0			*us*	
$\overline{CEI}$ High to Power Fail	t_{PF}	0			ns	

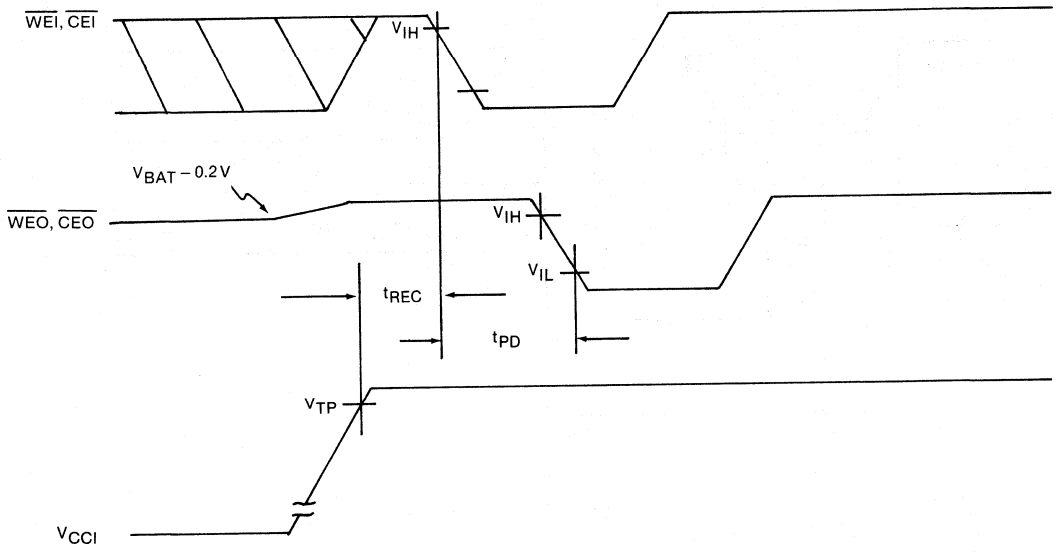
TIMING DIAGRAM—SWITCH SETTING



TIMING DIAGRAM—POWER DOWN



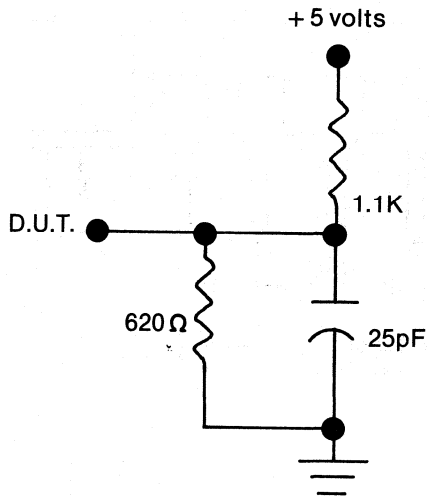
TIMING DIAGRAM—POWER UP

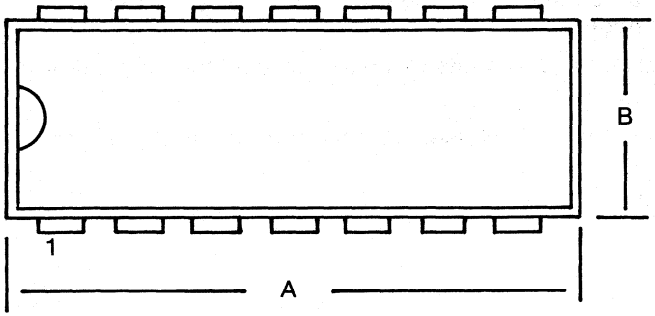


NOTES:

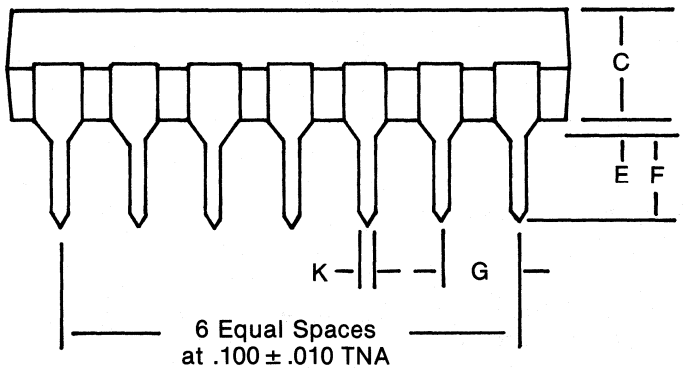
1. All voltages are referenced to ground.
2. Measured with V_{CCO}, $\overline{CE0}$ and $\overline{WE0}$ open.
3. I_{CCO} is the maximum average load which the DS1234 can supply to the memories.
4. Measured with a load as shown in Figure 2.
5. I_{CC01} is the maximum average load current which the DS1234 can supply to the memories in the battery back-up mode.
6. Chip Enable, $\overline{CEO}$, and Write Enable, $\overline{WEO}$, outputs can only sustain leakage current in the battery back-up mode.
7. I_{BAT} is the total load current which the DS1234 uses from the battery input pin with V_{CCO}, $\overline{CEO}$, and $\overline{WEO}$ open.

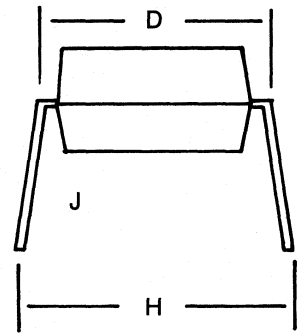
OUTPUT LOAD Figure 2





DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021





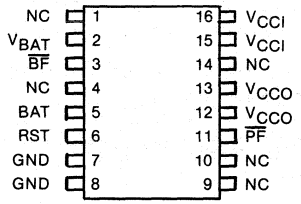
Dallas Semiconductor
Battery Manager

DS1259

FEATURES

- Facilitates uninterruptable power
- Uses battery only when primary V_{CC} is not available
- Low forward voltage drop
- Power fail signal interrupts processor or write protects memory
- Consumes less than 100 nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when V_{CC} is applied
- Mates directly with DS1212 Controller to back up 16 RAMs

PIN CONNECTIONS



PIN NAMES

NC - No Connection
V_{BAT} - Battery Input Connection
$\overline{BF}$ - Battery Fail Output Signal
BAT - Battery Output
RST - Reset Ground Signal
GND - Ground
$\overline{PF}$ - Power Fail Output Signal
V_{CCO} - V_{CC} Outputs
V_{CCI} - V_{CC} Inputs

DESCRIPTION

The DS1259 is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V_{CCO} pins. When power is supplied from the battery, the power fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

OPERATION

During normal operation, V_{CCI} (Pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (Pins 13 and 14) through an internal switch at a voltage level of $V_{CCI} - 0.2$ volts@250 mA. During this time the power fail signal ($\overline{PF}$) is held high indicating valid V_{CCI} voltage (see Figure 1). However, if the V_{CCI} would fall below the trip point (V_{TP}), a level of 1.26 times the battery level (V_{BAT}), the power fail signal is driven low. As V_{CCI} falls below the battery level, power is switched from V_{CCI} to V_{BAT} and the battery supplies power to the uninterruptable output (V_{CCO}) at $V_{BAT}) - 0.2$ volts@15 mA.

On power up, as the V_{CCI} supply rises above the battery, the primary energy source, V_{CCI}, becomes the supply. As V_{CCI} rises above the trip point (V_{TP}), the power fail signal is driven back to the high level. During normal operation BAT (Pin 5) stays at the battery level regardless of the level of V_{CCI}.

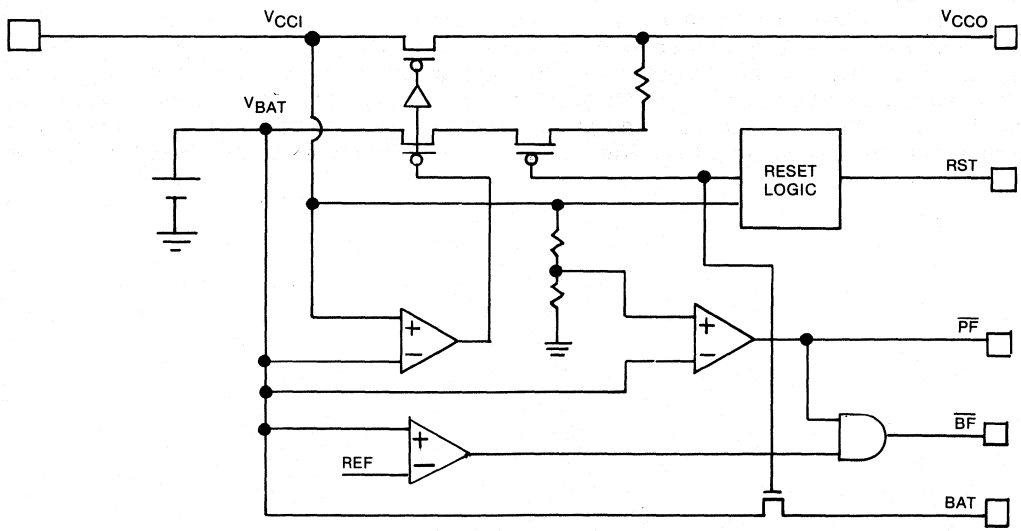
BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level provided that the attached battery (V_{BAT}) is greater than 2 volts. If the battery level should decrease to below 2 volts, the BF signal is driven low indicating a low battery. The $\overline{BF}$ signal is always low when the $\overline{PF}$ signal is low.

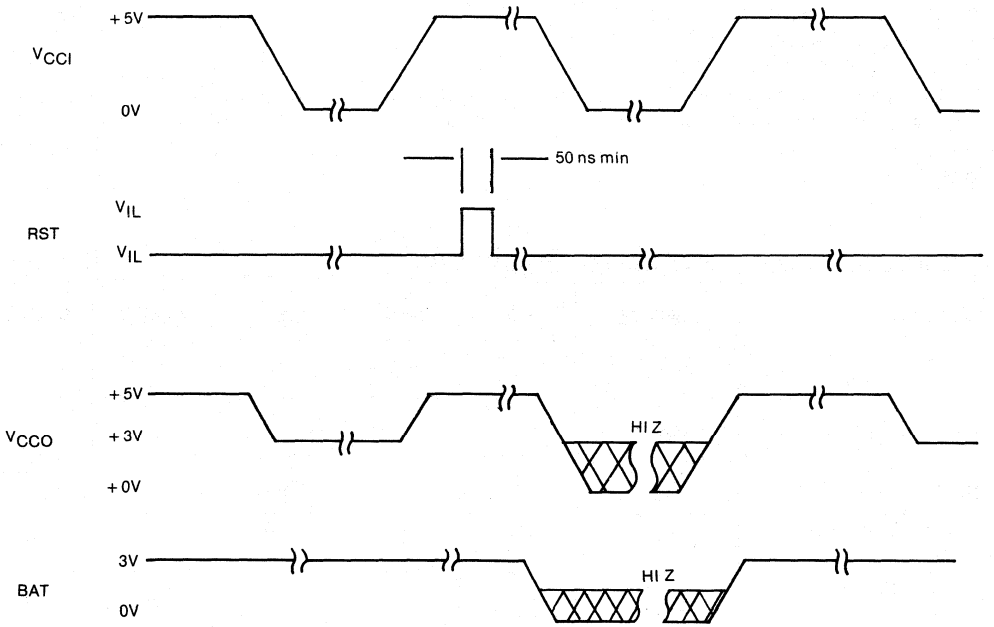
RESET

The reset input can be used to prevent the battery from supplying power to V_{CCO} and BAT even if V_{CCI} falls below the level of the battery. This feature is activated by applying a pulsed input on RST to high level for 50 ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to the high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the battery or V_{CCI}. The BAT output will also return to the level of the battery. Figure 3 shows the DS1259 in a typical application.

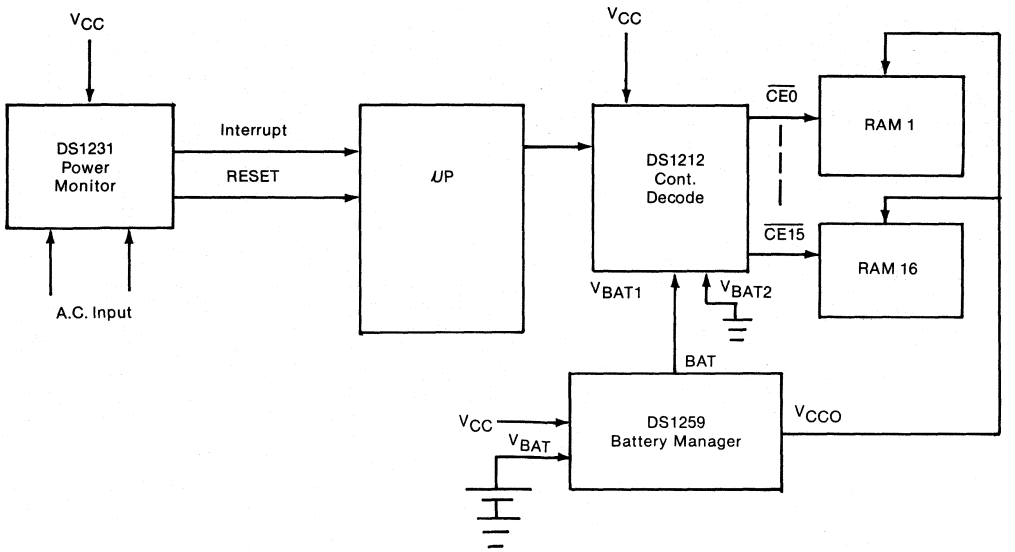
BLOCK DIAGRAM Figure 1



RESET TIMING Figure 2



TYPICAL APPLICATION Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}		5.0	5.5	V	1
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Input Low Voltage	V_{IL}	−0.3		+0.8	V	1
Battery Voltage Pin 5	V_{BAT}	2.5	3	3.7	V	6
Battery Output Pin 5	BAT	$V_{BAT}-0.1$			V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	−1.0		+1.0	*u*A	
Output Current @2.4V	I_{OH}	−1.0			mA	1,2
Output Current @0.4V	I_{OL}			+4.0	mA	1,2
Input Supply Current	I_{CCI}			10	mA	3
Pins 12, 13 V_{CCO} $V_{CCI}-0.2$	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}		1.26*X* V_{BAT}		V	4,6
Pin 3 $\overline{BF}$ Detect	V_{BATF}		2.0		V	7

(0 °C to 70 °C, $V_{CCI} < V_{BAT}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pins 12, 13 V_{CCO} $V_{BAT} - 0.2V$	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8
Pin 5 Battery Output Current	$I_{BAT\ OUT}$			100	uA	

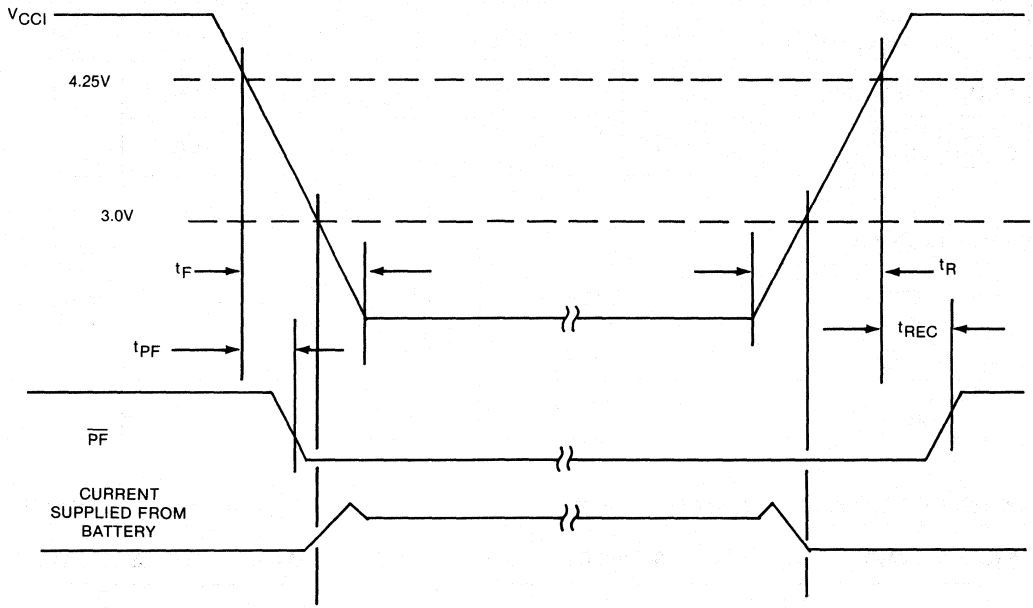
CAPACITANCE ($t_A = 25$ °C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Output Capacitance	C_{OUT}	5	10	pF

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 4.0$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			us	
V_{CCI} Slew Rate	t_R	1			us	
Power Down to $\overline{PF}$ Low	t_{PF}	0			us	
$\overline{PF}$ High after Power Up	t_{REC}			100	us	

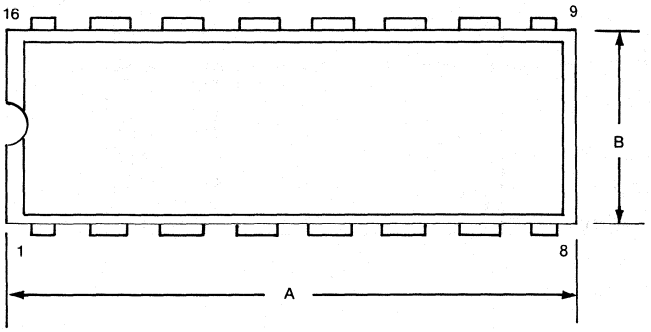
POWER-DOWN/POWER-UP CONDITION



NOTES:

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13 and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. I_{CCO2} may be limited by the capability of the battery.
6. Trip Point Voltage for Power Fail Detect:
   $V_{TP} = 1.26 \times V_{BAT}$
   For 5% operation: $V_{BAT} = 3.7V$ Max.
7. V_{BATF} is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1259.

DS1259
Battery Manager



DIM.	INCHES	
	MIN.	MAX.
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B	.240	.260
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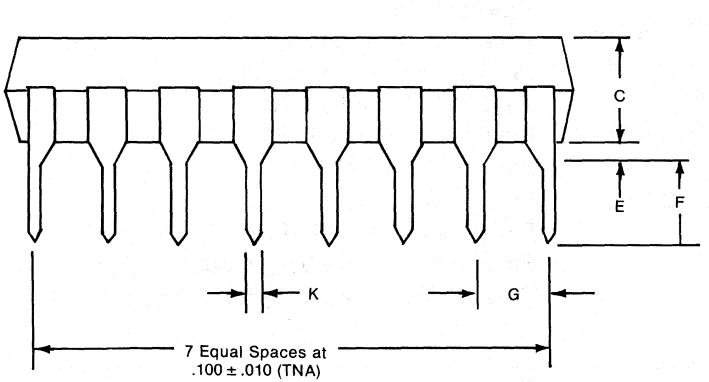
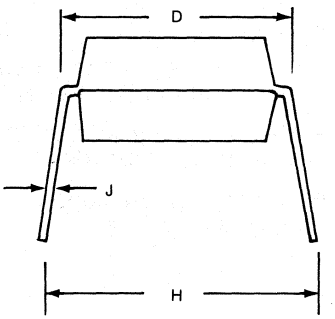
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021





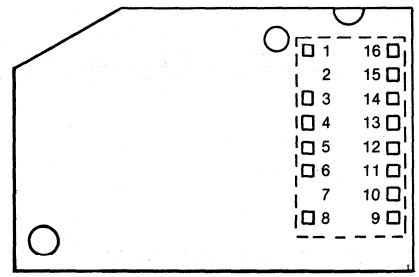
Dallas Semiconductor
SmartBattery

DS1260-25
-50
-100

FEATURES

- Encapsulated lithium energy cell with shelf life beyond 10 years
- Available with energy capacities of 250, 500, and 1,000 MAH @ 3 volts
- Plugs into a standard 16 pin DIP socket
- Lithium cell electrically disconnects from exposed pins upon command
- Battery isolation insures full capacity after shipping and handling
- Lithium cell automatically reconnects when V_{CC} is applied
- Recessed pins prevent bending
- V_{CC} fail signal interrupts processor or write protects memory
- Exhausted energy cell warning signal
- Low profile permits mounting on 0.5 inch printed circuit board centers
- Mates directly with DS1212 controller to back-up 16 SRAMs
- Uninterruptable supply for CMOS and portable devices

PIN CONNECTIONS



PIN NAMES

Pins, 1, 4, 9, 10 and 14 are No-Connects
Pin 2 and pin 7 are missing
Pin 3 is Battery Fail ($\overline{BF}$)
Pin 5 is Battery Out (BAT)
Pin 6 is RESET (RST)
Pin 8 is Ground
Pin 11 is Power Fail ($\overline{PF}$)
Pins 12 and 13 are V_{CC} Output (V_{CCO})
Pins 15 and 16 are V_{CC} Input (V_{CCI})

DESCRIPTION

The DS1260 is a low cost backup energy source for portable and nonvolatile electronic equipment. A lithium energy source of up to 1 amp hour can supply power to CMOS electronic circuits when primary power is lost through an intelligent and efficient switch. When power is supplied from the lithium power source, the power fail signal is held low to warn electronic RESET circuits of the power status. Energy loss during shipping and handling is avoided by pulsing RESET, thereby causing the backup energy source to be isolated from the exposed pins. The DS1260 can be plugged into a standard 16-pin low-cost DIP socket, allowing for proven interconnect and simple replacement if the energy has been exhausted.

OPERATION

During normal operation V_{CCI} (Pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (Pins 13 and 14) through an internal switch at a voltage level of $V_{CCI} - 0.2$ volts @ 250 ma. During this time the power fail signal $\overline{PF}$ is held high indicating valid primary voltage (see Figure 1). However, if the V_{CCI} would fall below the level of 4.25 volts, the power fail signal is driven low. As V_{CCI} falls below the level of the lithium supply ($V_{BAT} = 3$ volts) power is switched and the lithium energy source supplies power to the uninterruptable output (V_{CCO}) at $V_{BAT} - 0.2$ volts @ 5 MA.

On power up, as the V_{CCI} supply rises above 3 volts, the primary energy source, V_{CCI}, becomes the supply. As the V_{CCI} input rises above 4.25 volts the power fail signal is driven back to the high level. During normal operation BAT (Pin 5) stays at the battery level of 3 volts, regardless of the level of V_{CCI}.

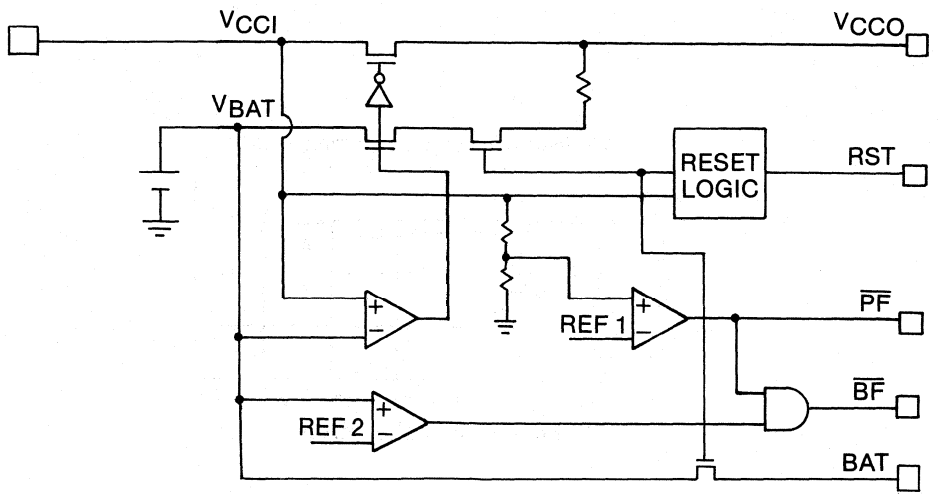
BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level (V_{OH}) provided that the lithium energy source is greater than 2 volts. If the lithium energy source should decrease to below 2 volts, the $\overline{BF}$ signal is driven low (V_{OL}), indicating an exhausted lithium battery. The $\overline{BF}$ signal is always low when power is being supplied by the lithium energy source.

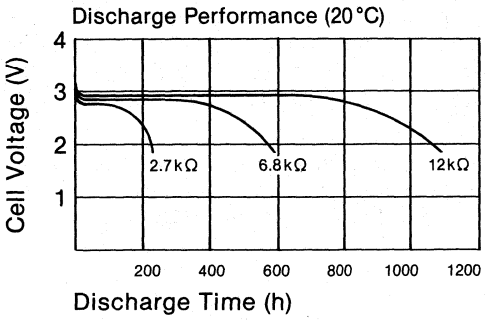
RESET

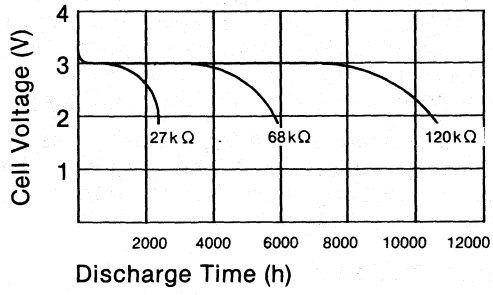
The reset input can be used to prevent the lithium energy source from supplying power to V_{CCO} and BAT even if V_{CCI} falls below 3 volts. This feature is activated by applying a pulsed input on RST to high level (V_{IH}) for 50 ns min. while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied, such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the lithium energy source when V_{CCI} again falls below 3 volts. BAT will also return to the level V_{BAT}. Figure 3 shows how the SmartBattery is used in a system application.

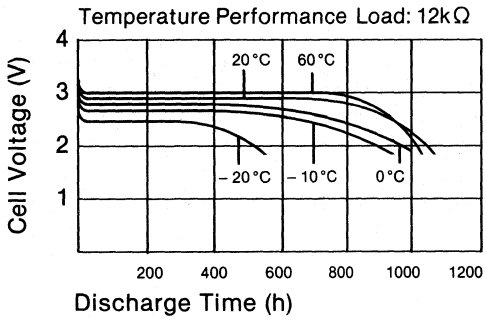
BLOCK DIAGRAM Figure 1

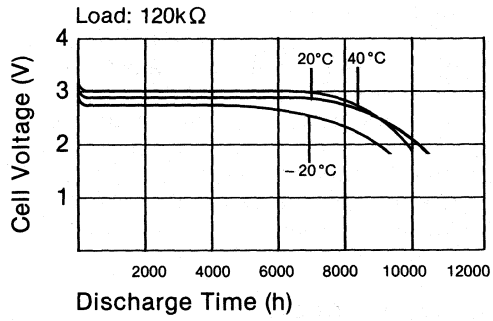


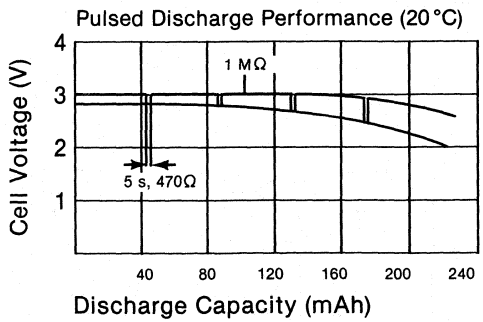
BATTERY PERFORMANCE DS1260-25



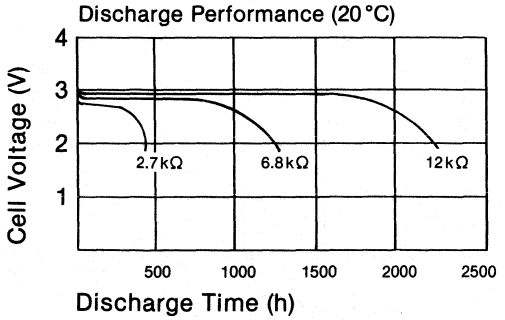


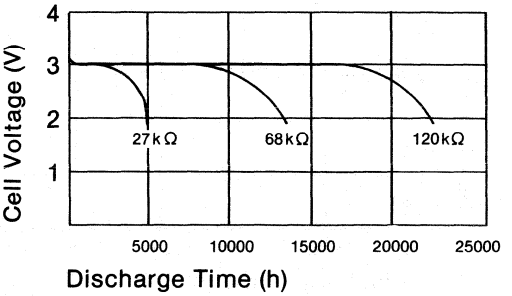


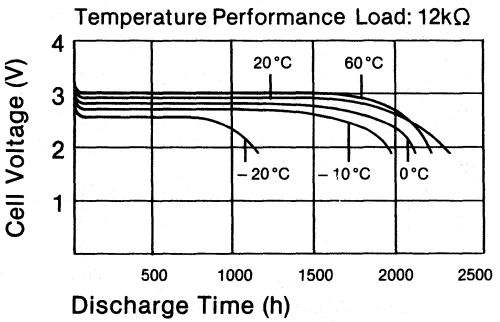


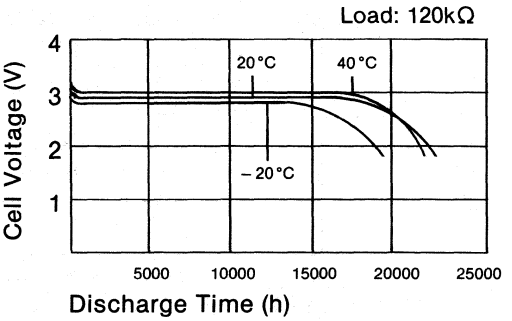


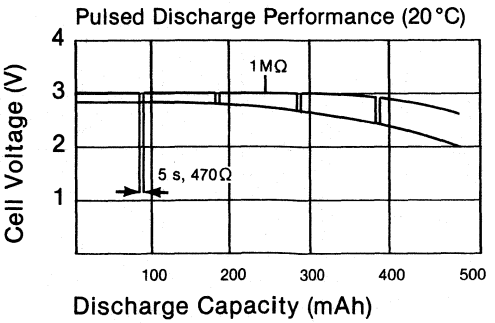
BATTERY PERFORMANCE DS1260-50



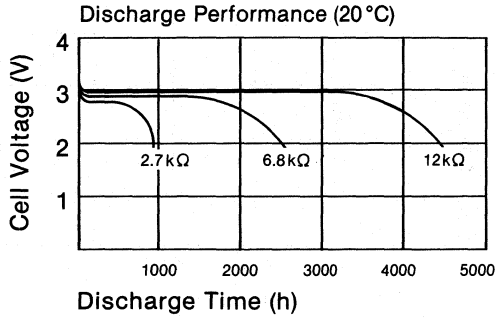


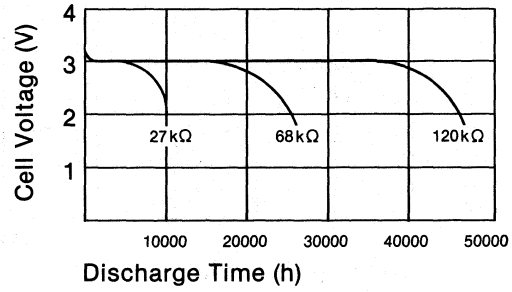


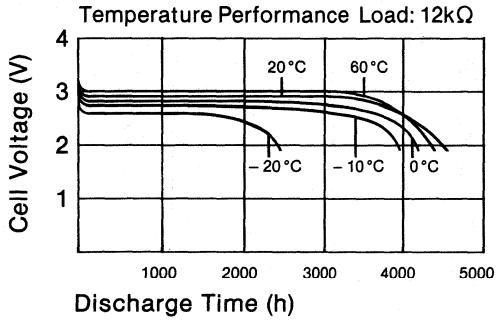


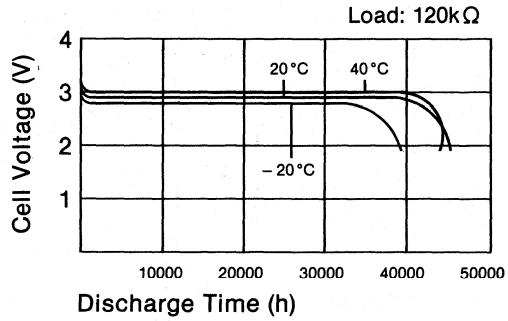


BATTERY PERFORMANCE DS1260-100









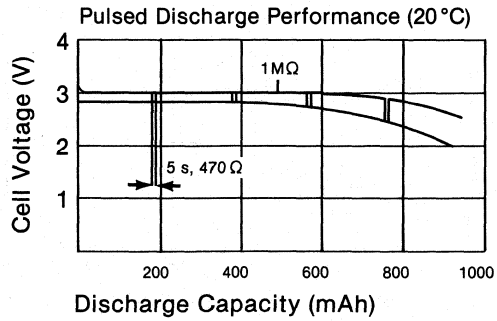
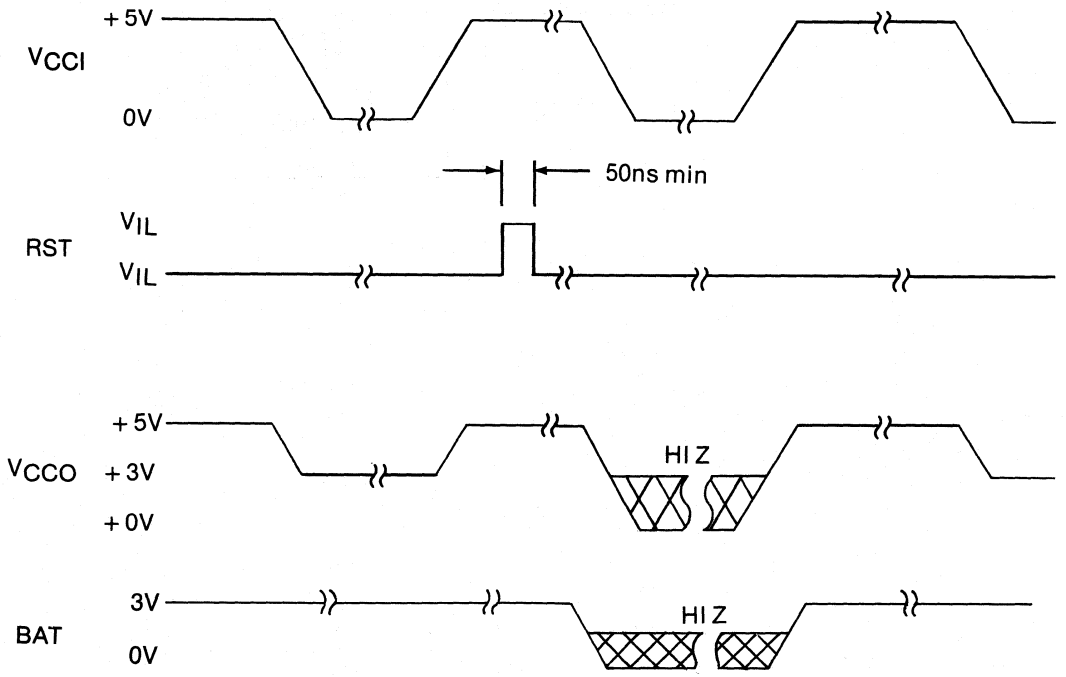


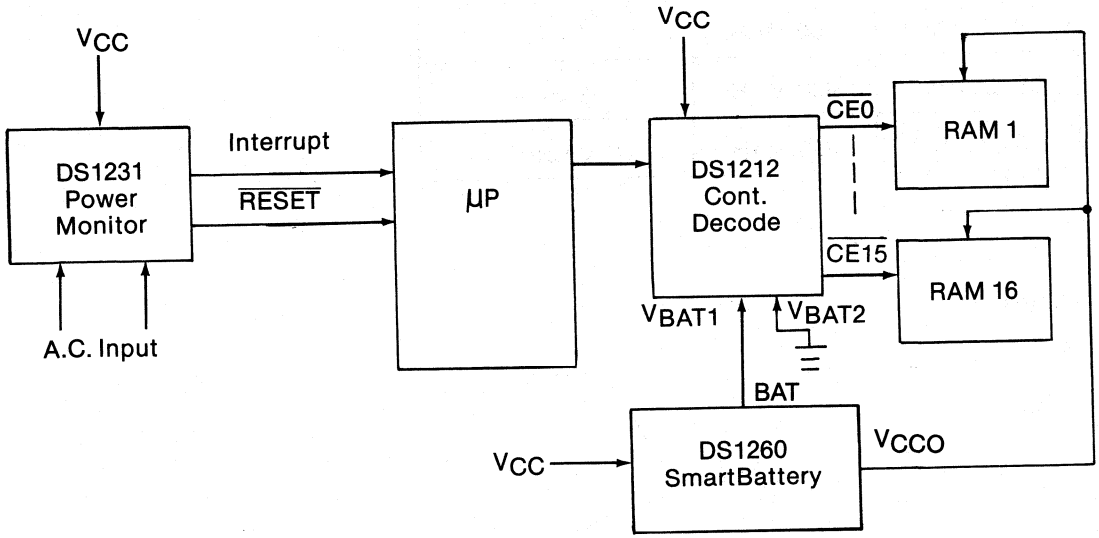
TABLE I

PART NO.	CAPACITY	NOMINAL VOLTAGE
DS1260-25	250 MAH	3 volts
DS1260-50	480 MAH	3 volts
DS1260-100	960 MAH	3 volts

FIGURE 2



INTEGRATED BATTERY BACKUP—APPLICATIONS Figure 3



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−0.3V to +7.0V
OPERATING TEMPERATURE	—	0°C to 70°C
STORAGE TEMPERATURE	—	−40°C to +70°C
SOLDERING TEMPERATURE	—	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}		5.0	5.5	V	1
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Input Low Voltage	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C V_{CCI} = 4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Leakage Current	I_{LO}	−1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	−1.0			mA	1,2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1,2
Input Supply Current	I_{CCI}			10	mA	3
Pins 12, 13 V_{CCO} $V_{CCI}-0.2$	I_{CCO}			250	mA	10
Pin 11 $\overline{PF}$ Detect	V_{TP}		4.25	4.5	V	4
Pin 3 $\overline{BF}$ Detect	V_{BATF}		2.0		V	7

(0°C to 70°C $V_{CCI} \leq V_{BAT}$)

Battery Voltage Pin 5	V_{BAT}		3		V	6
Pins 12, 13 $V_{CCO} \geq V_{BAT}-0.1V$	I_{CCO2}			5	mA	5
Battery Leakage	I_{BAT}			100	nA	8,9
Pin 5 Battery Output Current	$I_{BAT\ OUT}$			100	uA	

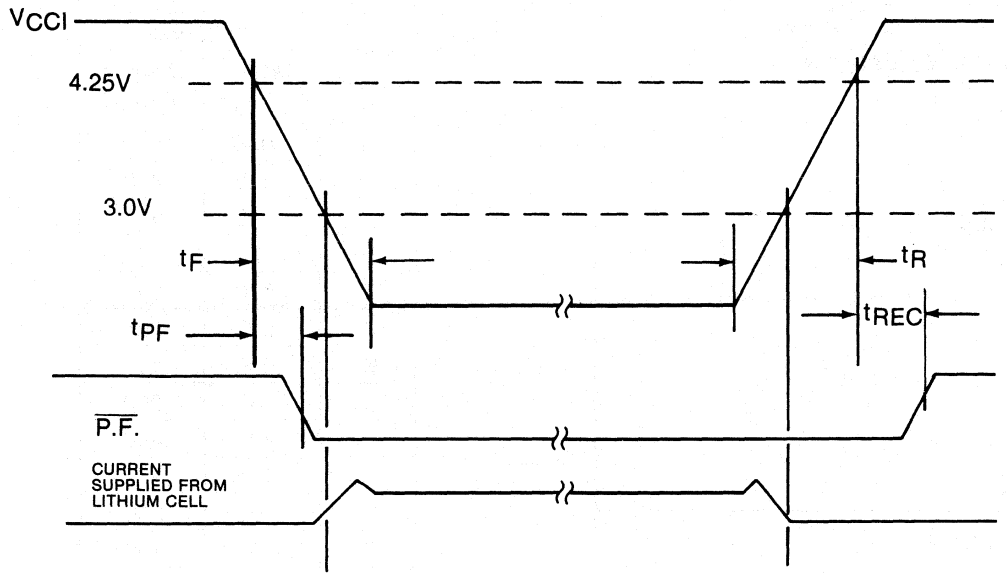
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Output Capacitance	C_O	5	10	pF
Input Capacitance	C_I	5	10	pF

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C V_{CC} = 4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	
V_{CCI} Slew Rate	t_R	1			µs	
Power Down to $\overline{PF}$ Low	t_{PF}	0			µs	
$\overline{PF}$ High after Power Up	t_{REC}			100	µs	

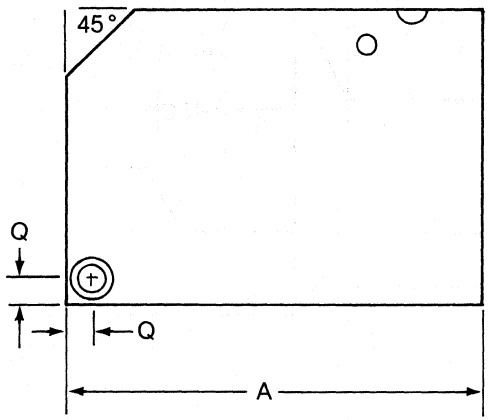
POWER-DOWN/POWER-UP CONDITION



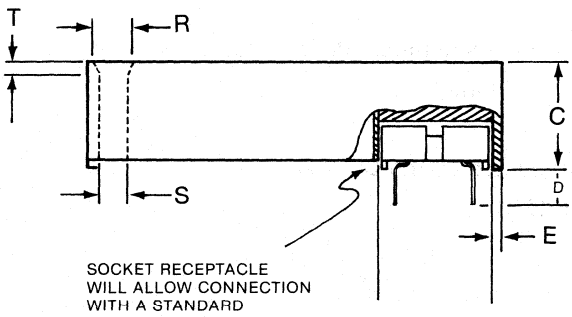
NOTES:

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13 and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. Sustained I_{CCO2} currents above 1 mA cause a significant drop in battery voltage.
6. V_{BAT} is the internal lithium energy source voltage.
7. V_{BATF} is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1260.
9. Storage loss is less than 1% per year at 25°C.
10. V_{CCI} = +5 volts; t_A = 25°C.

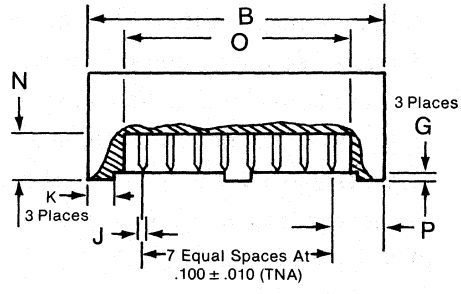
DS1260 - 25
- 50
- 100
SmartBattery



DIM.	INCHES	
	MIN.	MAX.
A	1.480	1.500
B	1.030	1.050
C	.390	.410
D	.120	.140
E	.020	.040
G	.020	.040
J	.022	.026
K	.090	.110
L	.240	.260
M	.420	.440
N	.165	.175
O	.800	.810
P	.160	.180
Q	.098	.109
R	.165	.175
S	.115	.125
T	.052	.058



SOCKET RECEPTACLE
WILL ALLOW CONNECTION
WITH A STANDARD
16 DIP SOCKET.
BURNDY DILB16P.-11T
SUPPLIED WITH EACH ORDER.



SOCKET NOT SHOWN

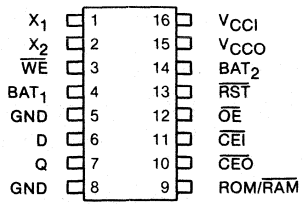
Dallas Semiconductor
TimeKeeper

PRELIMINARY
DS1215

FEATURES

- TimeKeeper keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backing up RAM
- Supports redundant batteries for high-rel applications
- Uses a 32.768 KHz watch crystal
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Space saving 16-pin DIP package

PIN CONNECTIONS



PIN NAMES

Pins 1 & 2	-	X_1, X_2	- 32.768 KHz Crystal Connections
Pin 3	-	$\overline{WE}$	- Write Enable
Pin 4	-	BAT_1	- Battery 1 Input
Pins 5 & 8	-	GND	- Ground
Pin 6	-	D	- Data In
Pin 7	-	Q	- Data Out
Pin 9	-	ROM/ $\overline{RAM}$	- ROM-RAM Select
Pin 10	-	$\overline{CEO}$	- Chip Enable Out
Pin 11	-	$\overline{CEI}$	- Chip Enable Input
Pin 12	-	$\overline{OE}$	- Output Enable
Pin 13	-	$\overline{RST}$	- Reset
Pin 14	-	BAT_2	- Battery 2 Input
Pin 15	-	V_{CCO}	- +5V Output
Pin 16	-	V_{CCI}	- +5V DC Input

DESCRIPTION

The DS1215 is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch provides hundredths of seconds, seconds, minutes, hours, day, date, month, and year information, while the nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

The last date of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator, or a 24-hour mode.

The nonvolatile memory controller portion of the circuit is designed to handle power fail detection, memory write protection, and battery redundancy. In short, the controller changes standard CMOS memories into nonvolatile memories, and provides continuous power to the TimeKeeper. Alternatively the TimeKeeper can be used with ROM memory by controlling the Chip Enable Output signal ($\overline{CEO}$) while the TimeKeeper is being accessed.

OPERATION

The block diagram of Figure 3 illustrates the main elements of the TimeKeeper. Communication with the TimeKeeper is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on Data In (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the Chip Enable Output pin ($\overline{CEO}$).

After recognition is established, the next 64 read or write cycles either extract or update data in the TimeKeeper and Chip Enable Output remains high during this time, disabling the connected memory.

Data transfer to and from the TimeKeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the TimeKeeper starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the TimeKeeper. These 64 write cycles are used only to gain access to the TimeKeeper.

When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is *not* found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 1). With a correct match for 64 bits, the TimeKeeper is enabled and data transfer to or from the TimeKeeping registers may proceed. The next 64 cycles will cause the TimeKeeper to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CEI}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the TimeKeeper.

A 32,786 Hz quartz crystal, Seiko part no. DS-VT-200 or equivalent, can be directly connected to the DS1215 via pins 1 and 2 (X_1, X_2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF.

NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the TimeKeeper is determined by the level of the ROM/$\overline{\text{RAM}}$ select pin. When ROM/$\overline{\text{RAM}}$ is connected to ground, the controller is set to the RAM mode and performs the circuit functions required to make static CMOS RAM and the TimeKeeping function nonvolatile. First a switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.2 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS static RAM. The DS1215 also performs redundant battery control for high reliability. On power fail the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground. The DS1215 provides the function of safeguarding the TimeKeeper and RAM data by power fail detection and write protection. Power fail detection occurs when V_{CCI} falls below VTP which is equal to $1.26 \times V_{BAT}$. The DS1215 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than VTP, a comparator outputs a power fail signal to the control logic. The power fail signal forces the chip enable output ($\overline{\text{CEO}}$) to V_{CCI} or $V_{BAT} - 0.2$ volts for external RAM write protection. During nominal supply conditions, $\overline{\text{CEO}}$ will track $\overline{\text{CEI}}$ with a maximum propagation delay of 20 ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the TimeKeeper registers and prevents future access until V_{CCI} exceeds VTP. A typical RAM/TimeKeeper interface is illustrated in Figure 4.

When the ROM/$\overline{\text{RAM}}$ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device which retains data in the absence of power, battery backup and write protection is not required. As a result, V_{CCO} is not switched to the battery and the chip enable logic will not force $\overline{\text{CEO}}$ high when power fails. However, the TimeKeeper does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power fail as V_{CCI} falls below the level of V_{BAT}. A typical ROM/TimeKeeper interface is illustrated in Figure 5.

TIMEKEEPER COMPARISON REGISTER DEFINITION Figure 1

	7	6	5	4	3	2	1	0	
Byte 0	1	1	0	0	0	1	0	1	C5
Byte 1	0	0	1	1	1	0	1	0	3A
Byte 2	1	0	1	0	0	0	1	1	A3
Byte 3	0	1	0	1	1	1	0	0	5C
Byte 4	1	1	0	0	0	1	0	1	C5
Byte 5	0	0	1	1	1	0	1	0	3A
Byte 6	1	0	1	0	0	0	1	1	A3
Byte 7	0	1	0	1	1	1	0	0	5C

NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the timekeeper is less than 1 in 10^{19}.

TIMEKEEPER REGISTER INFORMATION
The TimeKeeper information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the TimeKeeper registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the TimeKeeper registers are not binary coded decimal format (BCD) in 12-hour mode. Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

TIMEKEEPER REGISTER DEFINITION Figure 2

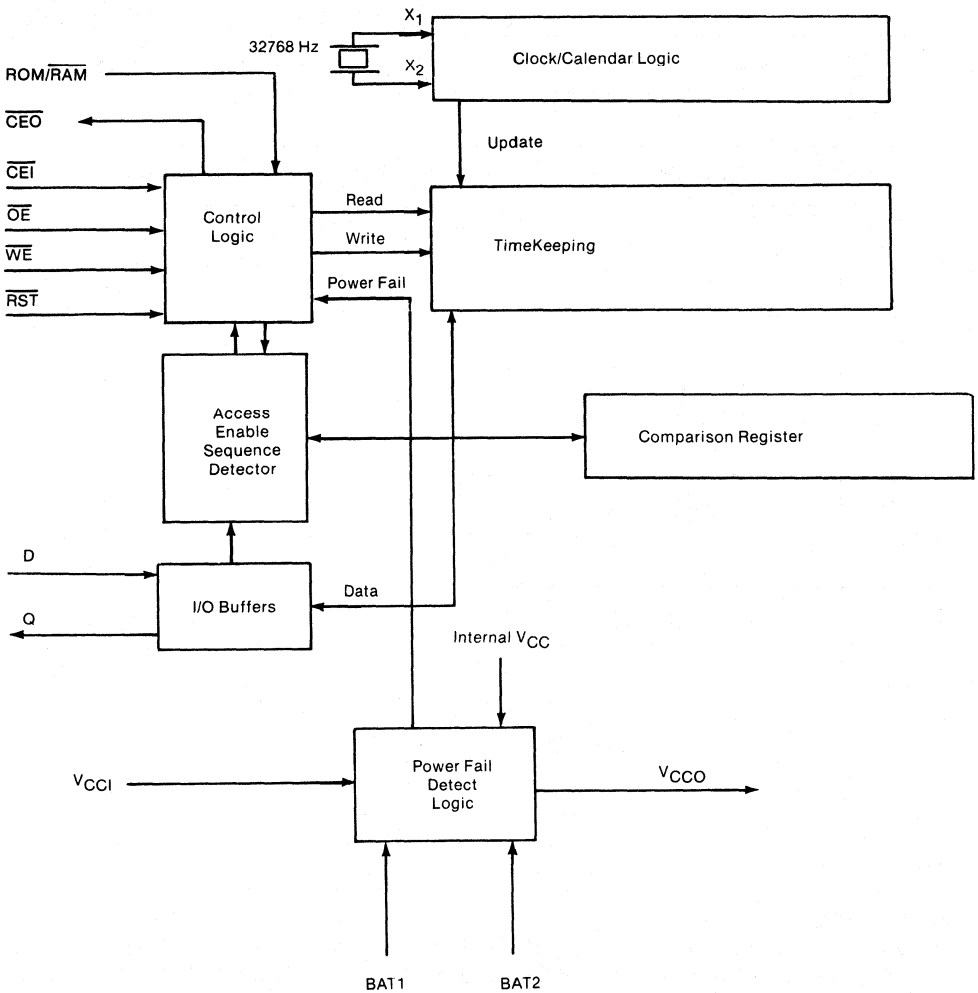
Register	7	6	5	4	3	2	1	0	Range (BCD)
0	0.1 SEC				0.01 SEC				00-99
1	0	10 SEC			SECONDS				00-59
2	0	10 MIN			MINUTES				00-59
3	12/24	0	10 A/P	HR	HOUR				01-12 00-23
4	0	0	$\overline{OSC}$	$\overline{RST}$	0	DAY			01-07
5	0	0	10 DATE		DATE				01-31
6	0	0	0	10 MONTH	MONTH				01-12
7	10 YEAR				YEAR				00-99

AM-PM/12/24 MODE
Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

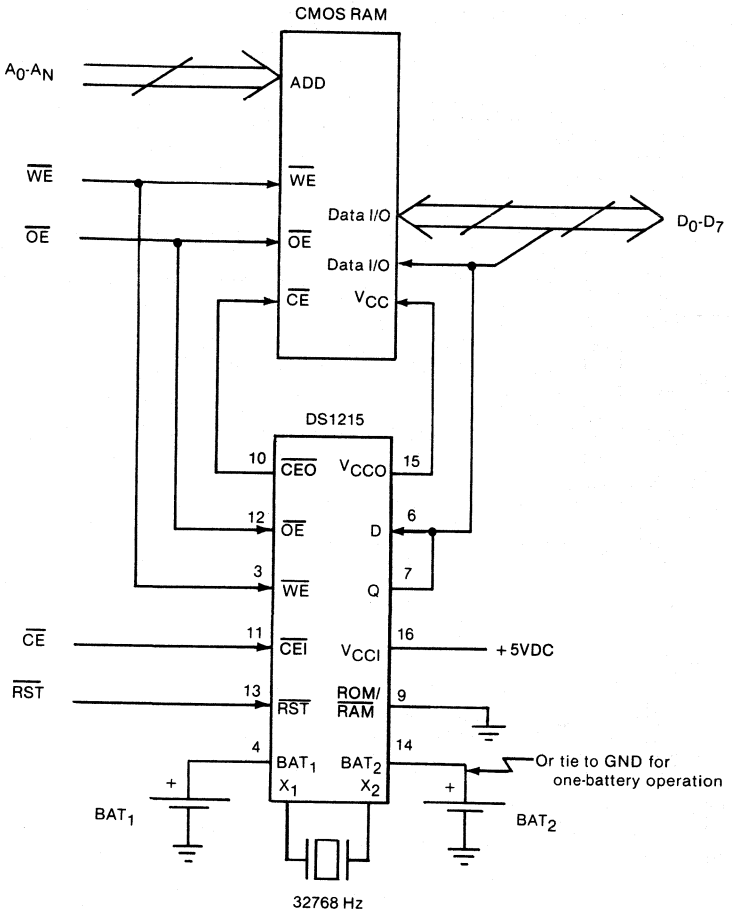
OSCILLATOR AND RESET BITS
Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logical 1, the reset input pin is ignored. When the reset bit is set to logical 0, a low input on the reset pin will cause the TimeKeeper to abort data transfer without changing data in the TimeKeeper registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to Logic 0 the oscillator turns on and the watch becomes operational.

ZERO BITS
Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

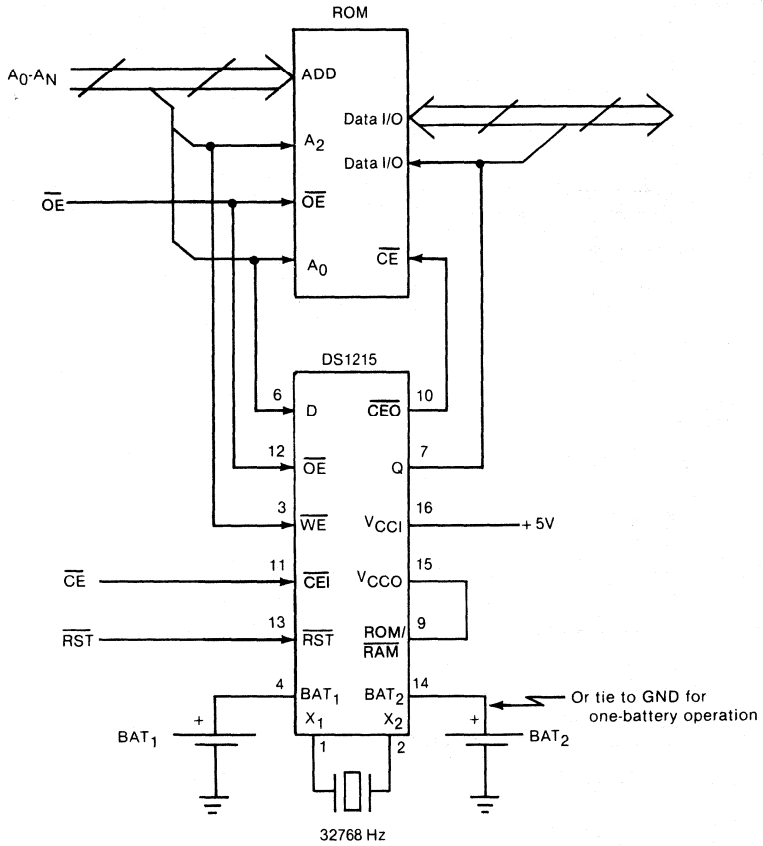
TIMEKEEPER BLOCK DIAGRAM Figure 3



RAM/TIMEKEEPER INTERFACE Figure 4



ROM/TIMEKEEPER INTERFACE Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 85°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	−0.3		+0.8	V	1
V_{BAT1} or V_{BAT2} Battery Voltage	V_{BAT}	2.5		3.7	V	7

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C V_{CC} = 4.5 to 5.5V)

Supply Current	I_{CCI}			5	mA	6
Supply Current $V_{CCO} = V_{CCI} - 0.2$	I_{CCO1}			80	mA	8
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
Output @2.4V	I_{OH}	−1.0			mA	2
Output @0.4V	I_{OL}			4.0	mA	2

(0°C to 70°C V_{CC} <4.5V)

$\overline{CEO}$ Output	V_{OH1}	V_{CC} or $V_{CC}-0.2$			V	9
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			1	uA	6
Battery Backup Current @$V_{CCO} = V_{BAT} - 0.2V$	I_{CCO2}			10	uA	10

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

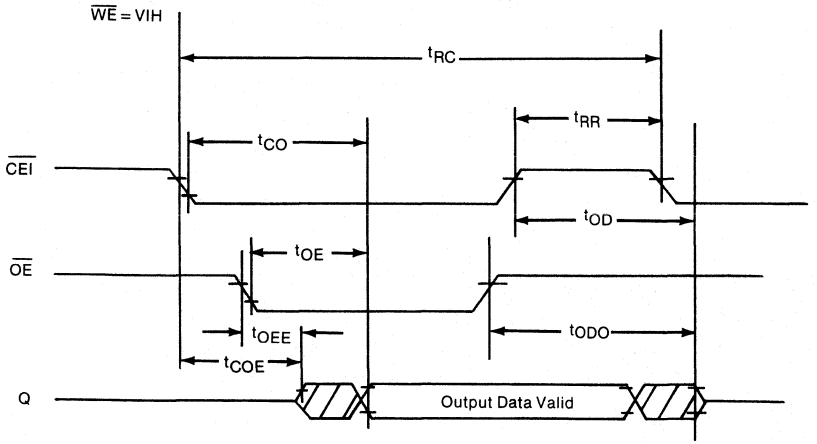
A.C. ELECTRICAL CHARACTERISTICS ROM/$\overline{\text{RAM}}$ = GND (0°C to 70°C V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{\text{CE}}$I Access Time	t_{CO}			200	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			100	ns	
$\overline{\text{CE}}$I To Output Low Z	t_{COE}	10			ns	
$\overline{\text{OE}}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{\text{CE}}$I To Output High Z	t_{OD}			100	ns	
$\overline{\text{OE}}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Set Up	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{\text{CE}}$I Pulse Width	t_{CW}	170			ns	
$\overline{\text{RST}}$ Pulse Width	t_{RST}	200			ns	
$\overline{\text{CE}}$I Propagation Delay	t_{PD}	5	10	20	ns	2, 3
$\overline{\text{CE}}$I High to Power Fail	t_{PF}			0	ns	

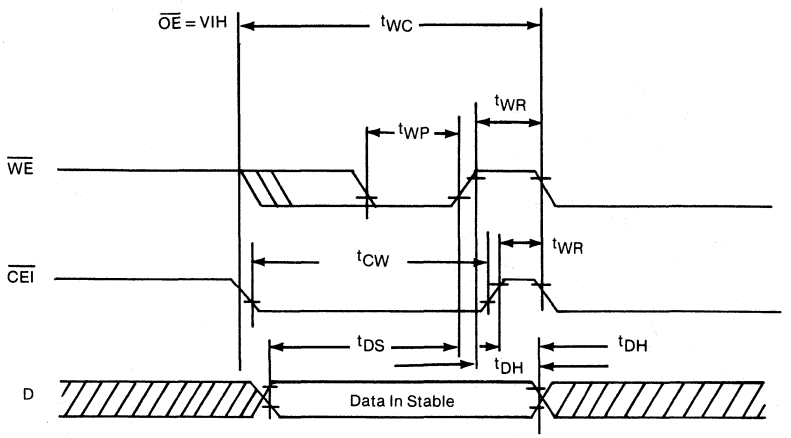
(0°C to 70°C V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

TIMING DIAGRAM—READ CYCLE TO TIMEKEEPER ROM/$\overline{\text{RAM}}$ = GND



TIMING DIAGRAM—WRITE CYCLE TO TIMEKEEPER ROM/$\overline{\text{RAM}}$ = GND



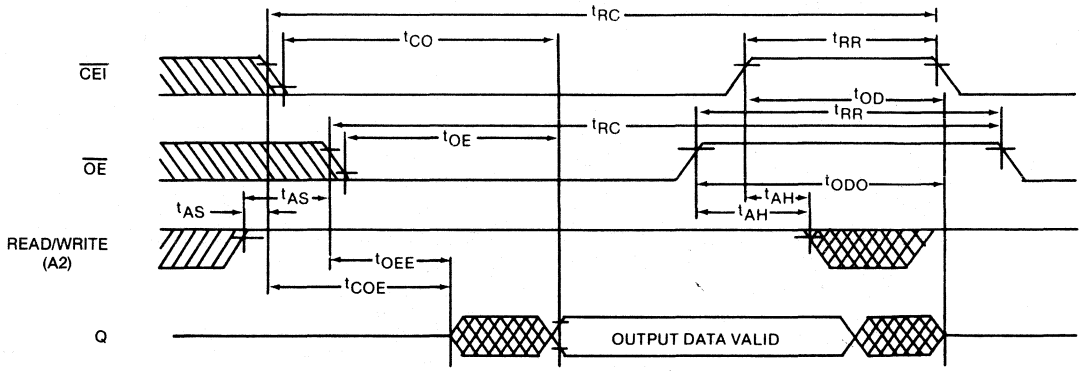
A.C. ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = V_{CCO} (0 °C to 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$I Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			200	ns	
$\overline{CE}$I to Output in Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{CE}$I to Output in High Z	t_{OD}			100	ns	
$\overline{OE}$ to Output in High Z	t_{ODO}			100	ns	
Address Set Up Time	t_{AS}	20			ns	
Address Hold Time	t_{AH}			10	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
$\overline{CE}$I Pulse Width	t_{CW}	170			ns	
$\overline{OE}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Set Up Time	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$I Propagation Delay	t_{PD}	5	10	20	ns	2,3
$\overline{CE}$I High to Power Fail	t_{PF}			0	ns	

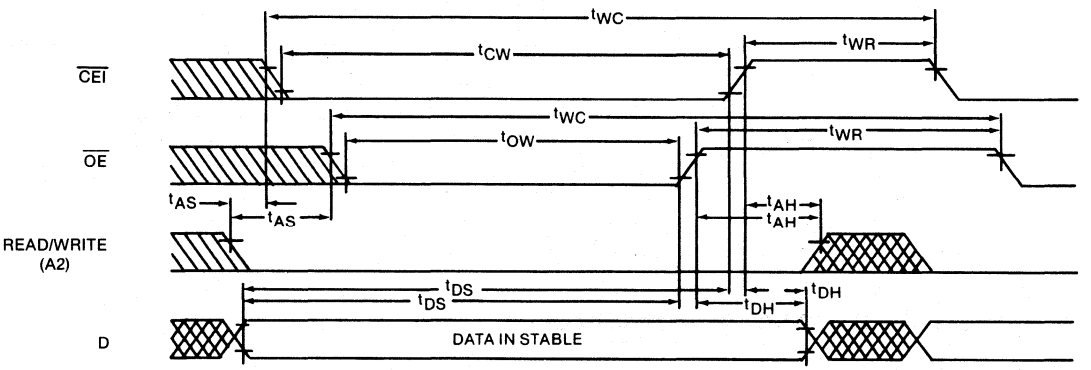
(0 °C to 70 °C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 -3V	t_F	0			ms	

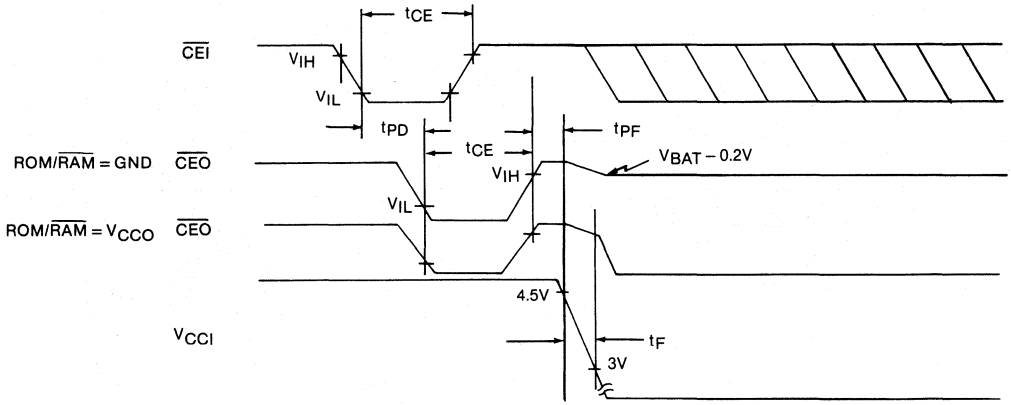
TIMING DIAGRAM—READ CYCLE ROM/$\overline{\text{RAM}}$ = V_{CCO}



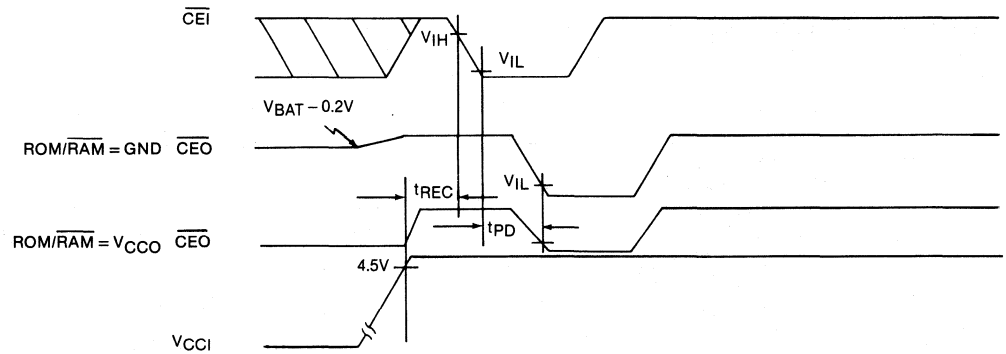
TIMING DIAGRAM—WRITE CYCLE ROM/$\overline{\text{RAM}}$ = V_{CCO}



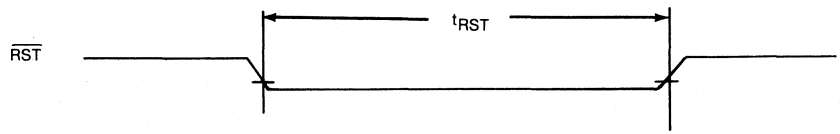
TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP



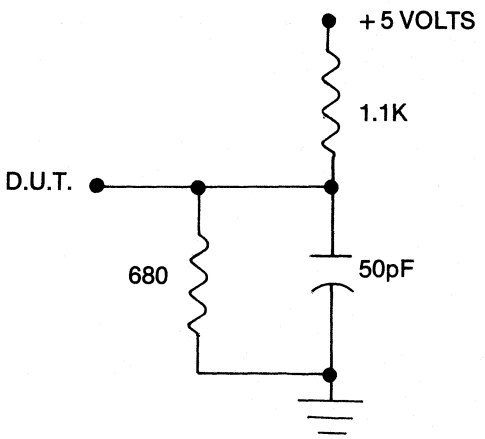
TIMING DIAGRAM—RESET FOR TIMEKEEPER



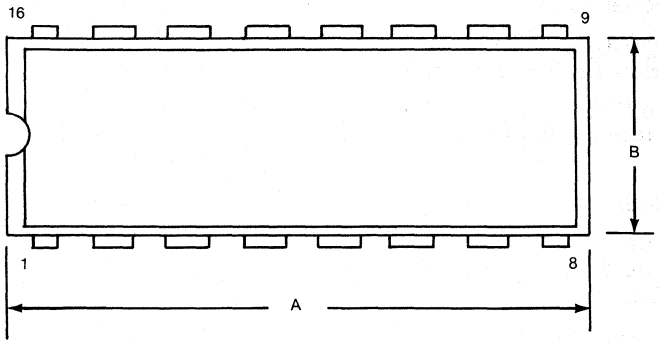
NOTES

1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10 ns.
4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power fail detect. $V_{TP} = 1.26 \times V_{BAT}$ For 10% operation $V_{BAT} = 3.5V$ max.; for 5% operation $V_{BAT} = 3.7V$ max.
8. I_{CCO1} is the maximum average load current the DS1215 can supply to memory.
9. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, $\overline{CEO}$ will go to a low level as V_{CCI} falls below V_{BAT}.
10. I_{CCO2} is the maximum average load current which the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to V_{CCI}.

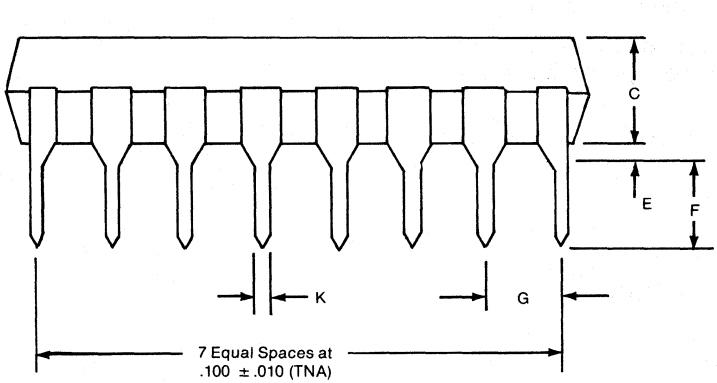
OUTPUT LOAD Figure 6

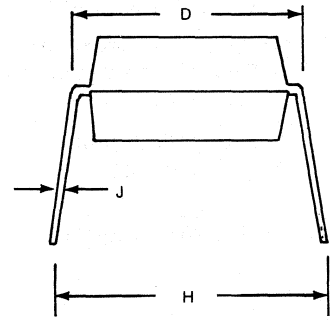


DS1215
TimeKeeper



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021





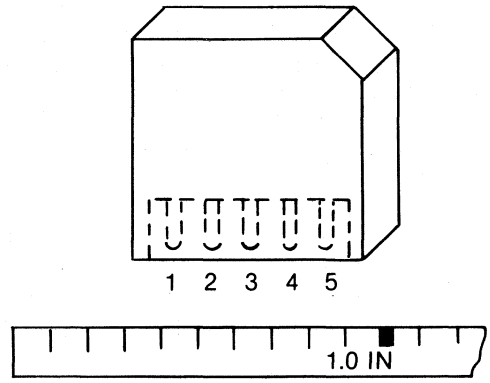
Dallas Semiconductor
Electronic Key

DS1204U

FEATURES

- Cannot be deciphered by reverse engineering
- Partitioned memory thwarts pirating
- User insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64 bit reprogrammable memory
- Unreadable 64 bit security match code virtually prevents deciphering by exhaustive search with over 10^{19} possibilities
- 128 bits of secure read/write memory creates additional barriers against hackers by permitting data changes as often as needed
- Rapid erasure of identification security match code, and secure read/write memory can occur if tampering is detected
- User insertable
- Over 10 years of data retention with no limitations or restrictions on write cycle
- Low power CMOS circuitry
- 4 million bits/second data rate
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN CONNECTIONS



PIN NAMES

Pin 1 — V_{CC}	+5 VOLTS
Pin 2 — $\overline{RST}$	$\overline{RESET}$
Pin 3 — DQ	DATA INPUT/OUTPUT
Pin 4 — CLK	CLOCK
Pin 5 — GND	GROUND

DESCRIPTION

The DS1204U Electronic Key is a miniature security system which stores 64 bits of user definable identification code and a 64 bit security match code which protects 128 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the key via a special program mode operation. After programming, the key follows a special procedure with a serial format to retrieve or update data.

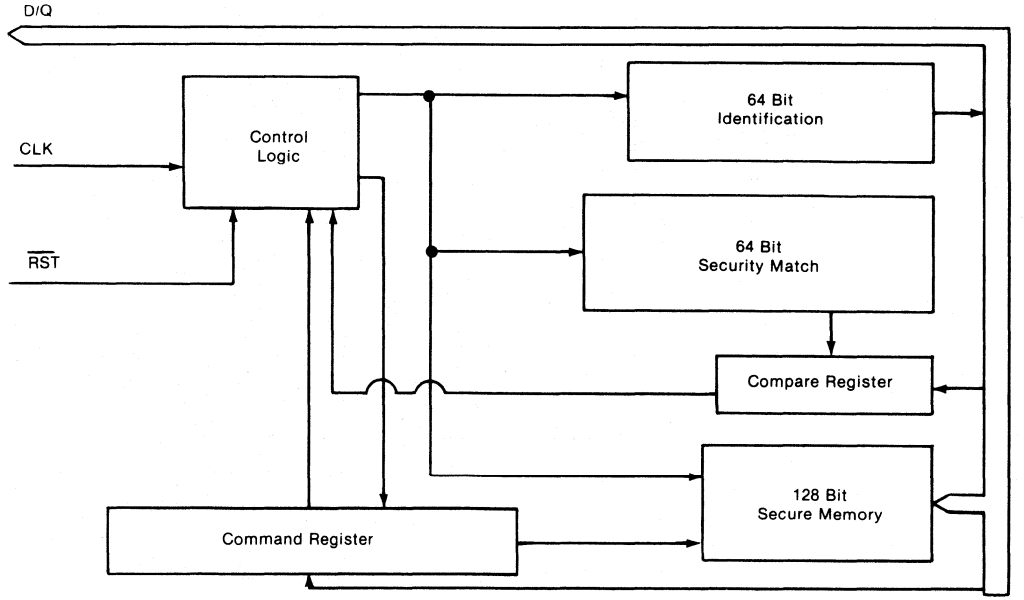
Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfer with only three signals: CLOCK, $\overline{\text{RESET}}$, and DATA INPUT/OUTPUT.

Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user insertable.

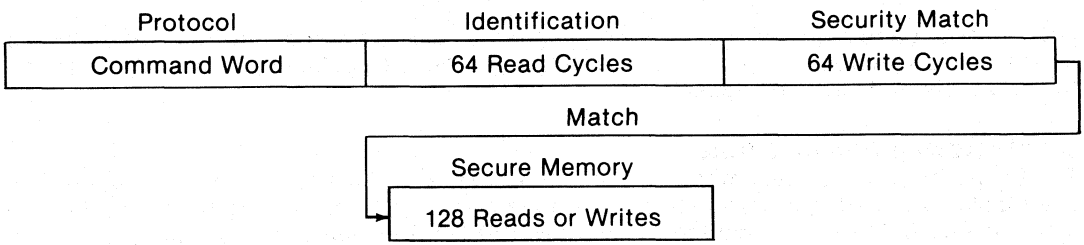
OPERATION—NORMAL MODE

The Electronic Key has two modes of operation: the normal mode and the program mode. The block diagram (Figure 1) illustrates the main elements of the key when used in the normal mode. To initiate data transfer with the key, $\overline{\text{RST}}$ is taken high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines normal operation for read or write or communications is ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the key are read. Data is clocked out of the key on the high to low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/write nonvolatile memory. Figure 2 is a summary of normal mode operation and Figure 3 is a flow chart of the normal mode sequence.

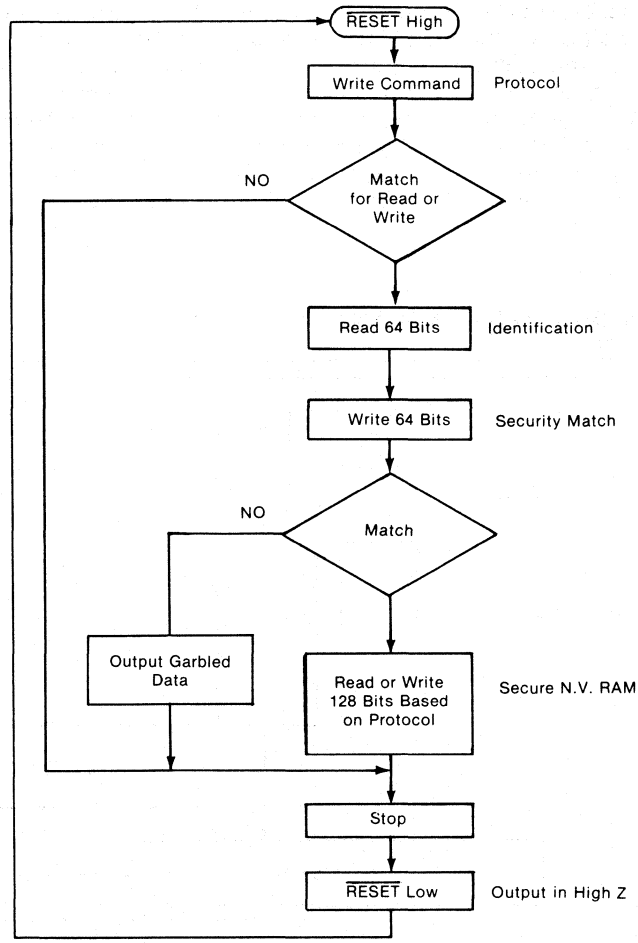
BLOCK DIAGRAM — NORMAL MODE Figure 1



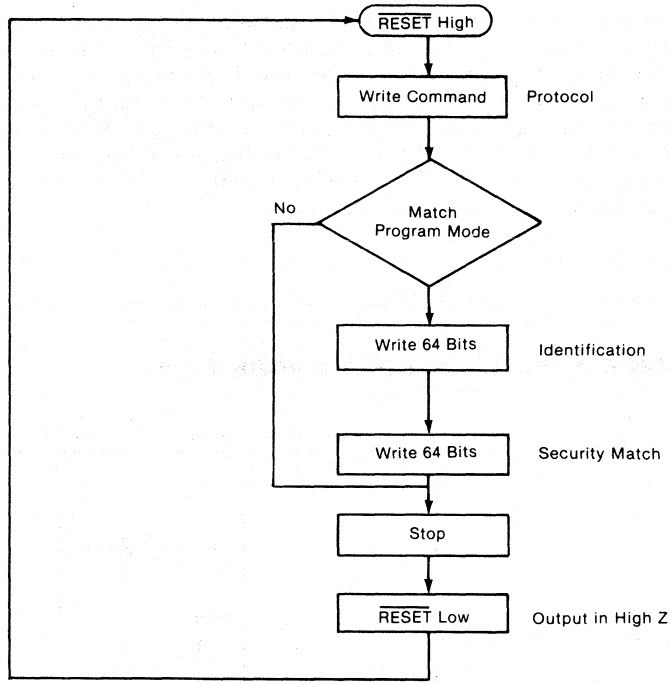
SEQUENCE — NORMAL MODE Figure 2



FLOW CHART — NORMAL MODE Figure 3



FLOW CHART — PROGRAM MODE Figure 6



COMMAND WORD

Each data transfer for the normal and program mode begins with a three byte command word as shown in Figure 7. As defined, the first byte of the command word specifies whether the 128 bit nonvolatile memory will be written into or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

The 8 bit pattern for read is 01100010. The pattern for write is 10011101. The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern which selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

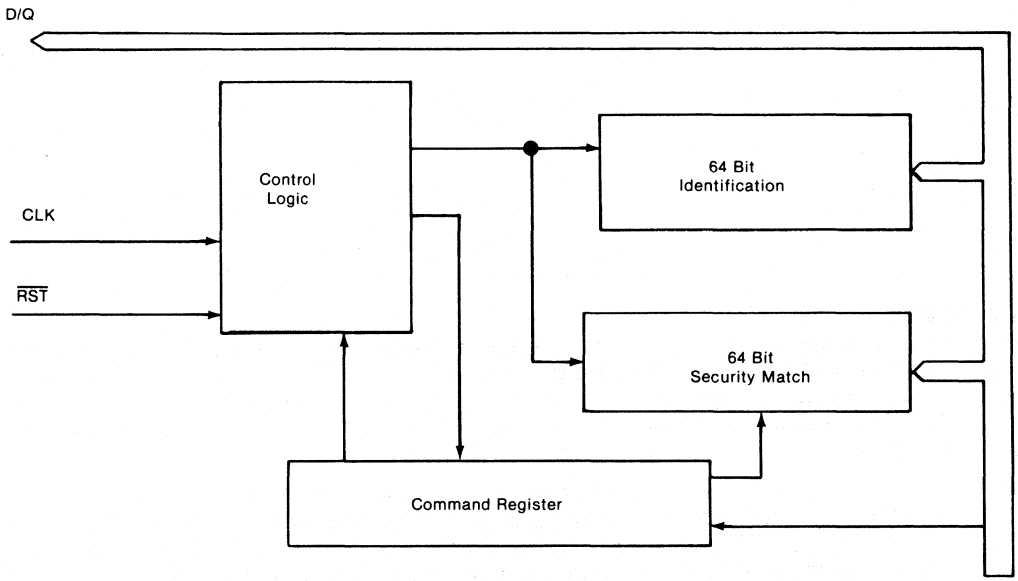
The remaining 6 bits of byte 2 and the first 7 bits of byte 3 form unique patterns which allow multiple keys to reside on a common bus. As such, each respective code pattern must be written exactly for a given device or data transfer will abort. Dallas Semiconductor has 5 patterns available as standard products per the chart in Figure 7. Each pattern corresponds to a specific part number. Under special contract with Dallas Semiconductor the user may specify any bit pattern other than that specified by Dallas Semiconductor as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

NOTE: Contact Dallas Semiconductor Sales Office for special command word code assignment which makes possible an exclusive blank key.

PROGRAM MODE

The block diagram of Figure 4 illustrates the main elements of the key when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact pattern which defines program operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, then the next 128 bits which follow are written to the identification memory and the security match memory. Figure 5 is a summary of program mode operation and Figure 6 is a flow chart of program mode operation.

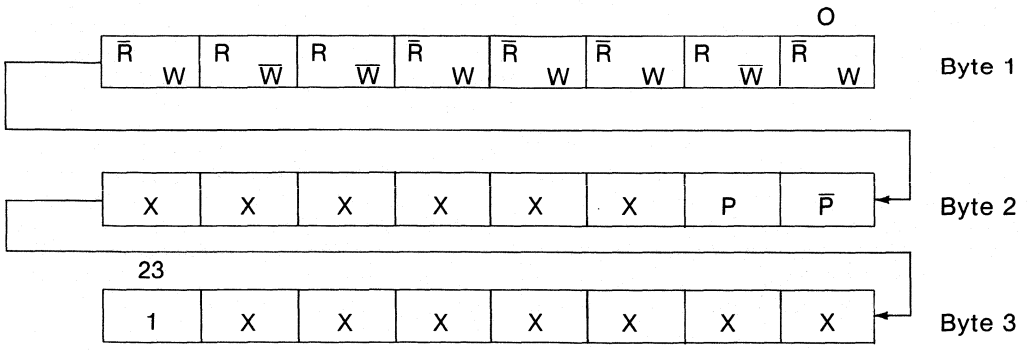
BLOCK DIAGRAM — PROGRAM MODE Figure 4



SEQUENCE — PROGRAM MODE Figure 5

Protocol	Identification	Security Match
Command Word	64 Write Cycles	64 Write Cycles

COMMAND WORD Figure 7



DS1204U-1	0	0	0	0	0	0	P	P̄	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-2	0	0	0	0	0	1	P	P̄	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-3	0	0	0	0	1	0	P	P̄	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-4	0	0	0	0	1	1	P	P̄	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-5	0	0	0	1	0	0	P	P̄	Byte 2
	1	0	1	0	0	0	0	0	Byte 3

RESET AND CLOCK CONTROL

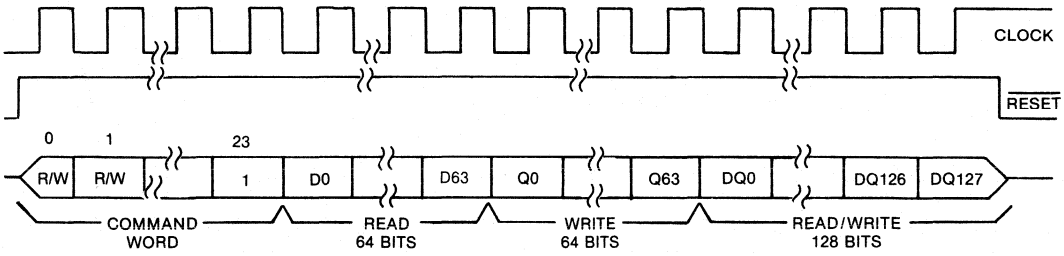
All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 mA @ 3.0 volts is required. However, if the V_{CC} pin is connected to a 5 volt source within nominal limits, then $\overline{RST}$ is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 uA. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. When data transfer to the key is terminated and using $\overline{RST}$, the transition of $\overline{RESET}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 8 for normal mode and Figure 9 for program mode.

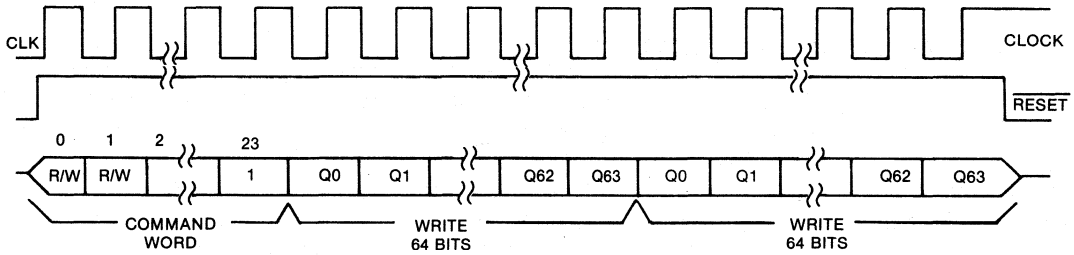
KEY CONNECTIONS

The key is designed to be plugged into a standard 5 pin 0.1 inch center SIP receptacle. A guide is provided to prevent the key from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the key pins can be determined to insure connection integrity before data transfer begins. CLK, $\overline{RST}$, and DATA INPUT/OUTPUT all have internal 20K Ohm pull down resistors to ground which can be sensed by a reading device.

DATA TRANSFER — NORMAL MODE Figure 8



DATA TRANSFER — PROGRAM MODE Figure 9



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to 70°C
STORAGE TEMPERATURE	—	−40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1,8,10
Logic 0	V_{IL}	−0.3		+0.8	V	1
$\overline{\text{RESET}}$ Logic 1	V_{IHE}	3.0			V	1,9,11
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	μA	4
Output Leakage	I_{LO}			+500	μA	
Output Current @ 2.4V	I_{OH}	−1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input Resistance	Z_{RST}	10		40	KΩ	
D/Q Input Resistance	Z_{DQ}	10		40	KΩ	
CLK Input Resistance	Z_{CLK}	10		40	KΩ	
$\overline{\text{RST}}$ Current @3.0V	I_{RST}			2	mA	6,9,13
Active Current	I_{CC1}			6	mA	6
Standby Current	I_{CC2}			1	mA	6

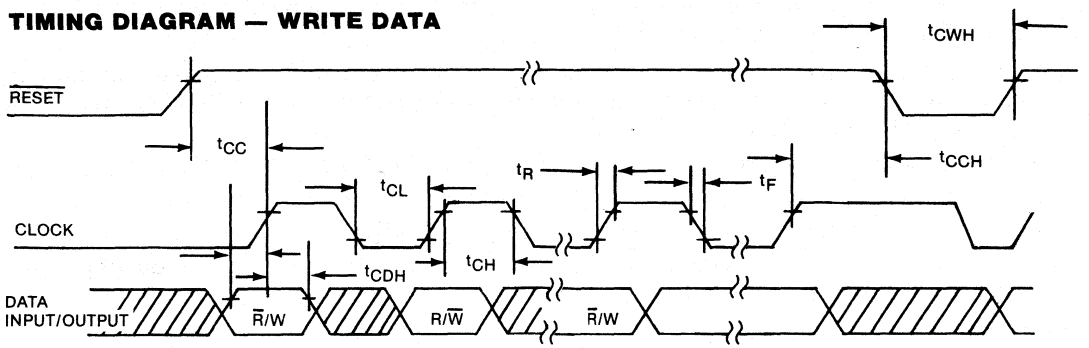
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

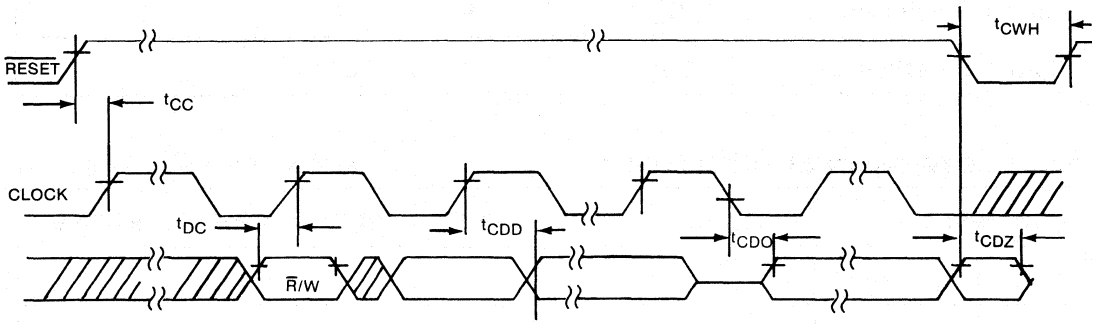
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70° $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	35			ns	2,7
CLK to Data Hold	t_{CDH}	40			ns	2,7
CLK to Data Delay	t_{CDD}			100	ns	2,3,5,7
CLK Low Time	t_{CL}	125			ns	2,7
CLK Low Time	t_{CH}	125			ns	2,7
CLK Frequency	f_{CLK}	D.C.		4.0	MHZ	2,7
CLK Rise & Fall	t_R, t_F			500	ns	2,7
$\overline{RST}$ To CLK Set Up	t_{CC}	1			us	2, 7
CLK To $\overline{RST}$ Hold	t_{CCH}	40			ns	2, 7
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	2,7,14
$\overline{RST}$ To I/O High Z	t_{CDZ}			50	ns	2, 7

TIMING DIAGRAM — WRITE DATA



TIMING DIAGRAM — READ DATA



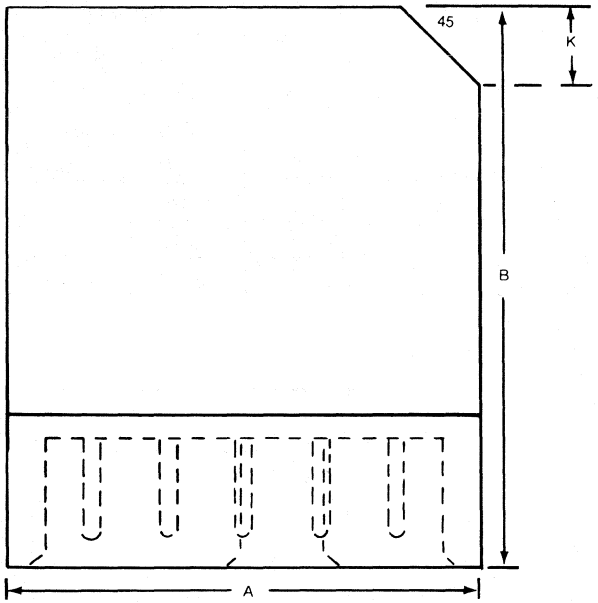
1. All voltages are referenced to GND.
2. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
3. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
4. For CLK, D/Q, and $\overline{RST}$
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of $\overline{RST} \geq 3.0V$ when $\overline{RST}$ supplies power.
8. Logic 1 maximum is $V_{CC} + 0.3$ volts if the V_{CC} pin supplies power and $\overline{RST} + 0.3$ volts if the $\overline{RST}$ pin supplies power.
9. Applies to $\overline{RST}$ when $V_{CC} < 3.0$ V.
10. Input levels apply to CLK, DQ, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the key, then $\overline{RST}$ input reverts to V_{IHE}.
11. $\overline{RST}$ Logic 1 maximum is $V_{CC} + 0.3$ volts if the V_{CC} pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1204U is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average A.C. $\overline{RST}$ current can be determined using the following formula:

    $I_{TOTAL} = 2 + I_{LOAD\ D.C.} + (4 \times 10^{-3})(C_L + 140)\ f$

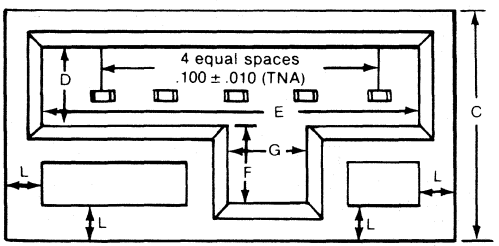
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHZ.

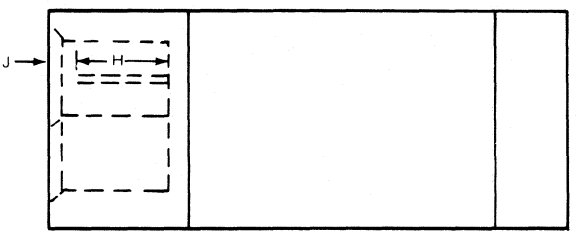
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHZ gives an I_{TOTAL} of 5 MA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to 10 μs.

Electronic Key
DS1204U

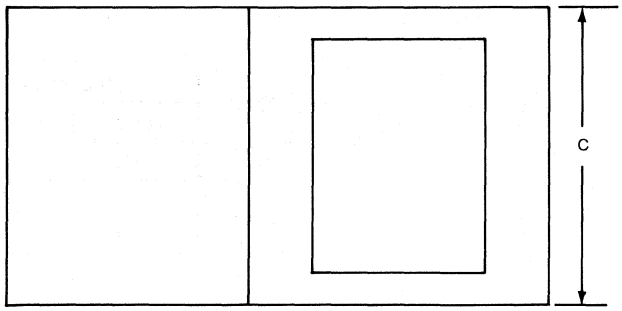


DIM.	INCHES	
	MIN.	MAX.
A	.610	.625
B	.745	.755
C	.310	.325
D	.100	.110
E	.515	.525
F	.100	.110
G	.100	.110
H	.110	.130
J	.030	.050
K	.045	.055
L	.045	.055

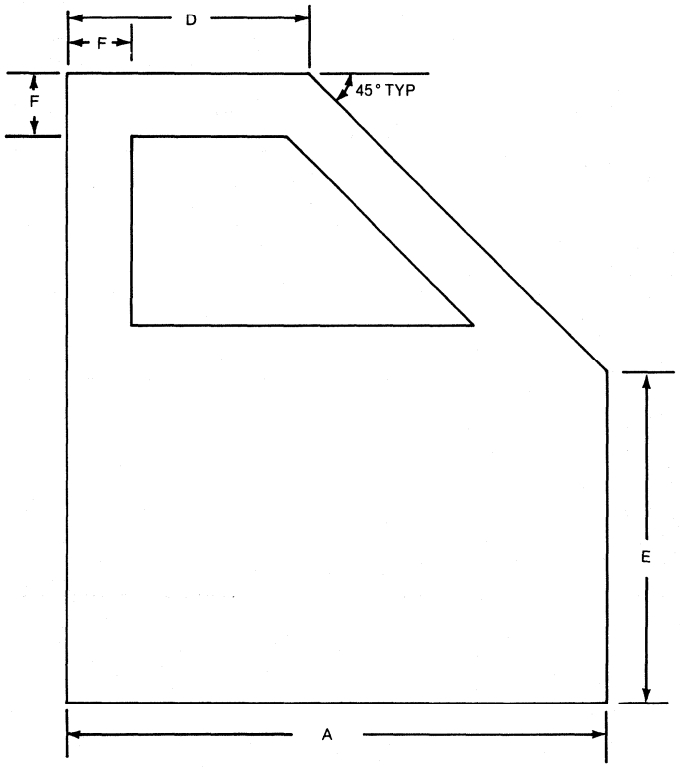


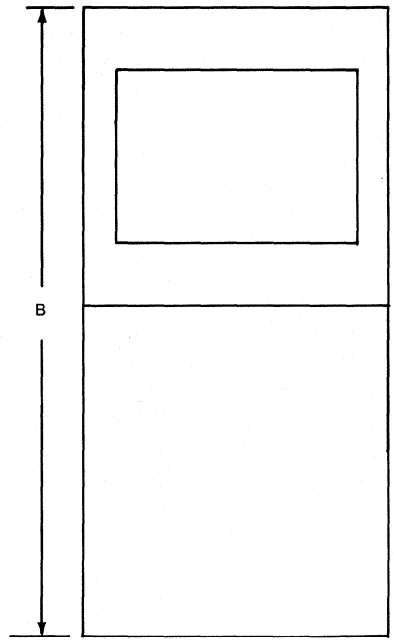


Key/Tag Holder
DS9090



DIM.	INCHES	
	MIN.	MAX.
A	.670	.690
B	.790	.810
C	.370	.390
D	.290	.310
E	.410	.430
F	.070	.090





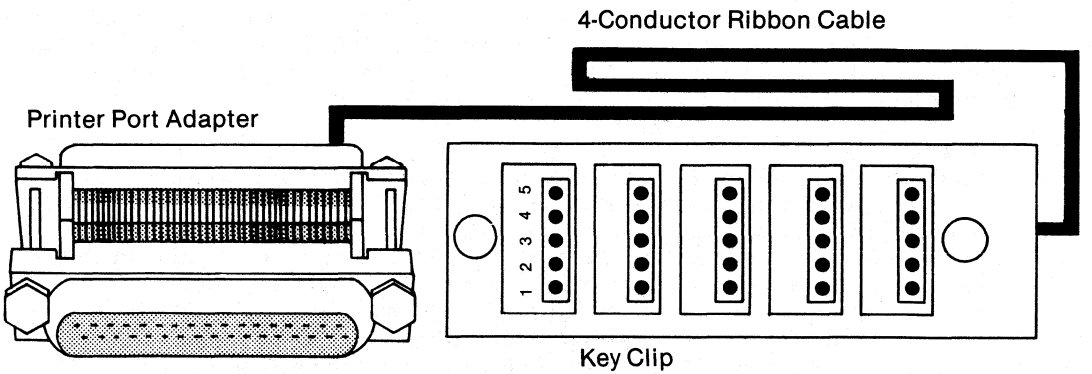
Dallas Semiconductor
Printer Port KeyRing — *DS1253*

FEATURES

- Low cost add on fixture for Electronic Keys, Tags, and TimeKeys
- Connects directly to IBM PC Parallel Printer Port without affecting printer operation
- Plug-in installation
- Key, Tag, and TimeKey communications are totally controlled by software
- Up to five Keys, Tags, and TimeKeys may be resident at one time
- Normal computer operation is unaffected
- Applications include software security, identification, personalization, and portable memory

PIN CONNECTIONS AND DEFINITIONS

Pin 1 - V_{CC} +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - D/Q - Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND Ground



DESCRIPTION

The DS1253 KeyRing adapts low pin count electronic Keys (DS1204U), Tags (DS1201S), and TimeKeys (DS1207) to the IBM PC Parallel Printer Port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the printer port adapter, and reconnecting the printer to back connector on the printer port adapter. The emanating 4-conductor ribbon cable can be routed such that the key clip can be attached to the computer cabinet in a convenient location with the adhesive provided. Up to 5 keys and/or tags can be inserted into the key clip at the same time. Communications with keys and tags occur under software control of the parallel printer port. The three control signals ($\overline{RESET}$, Clock, and Data In/Out) for Tags, Keys and TimeKeys are generated by consecutive I/O instructions which control the parallel printer port.

OPERATION

Keys, Tags, and TimeKeys have defined signal patterns which are required for communications. The signals $\overline{RST}$, CLK and DQ must be software controlled to duplicate the behavior as defined in the respective data sheet for Tags, Keys and TimeKeys. Each signal is a function of a specific output or I/O line of the printer port. Pin 4 on the 25-Pin D Connector Parallel Printer Port is called Data Out 2 (D2). This signal is used to provide $\overline{RST}$ for the KeyRing and must be kept at a high level when communicating with Tags, Keys, and TimeKeys. When $\overline{RST}$ is driven low all communication to Tags, Keys, and TimeKeys is terminated. The $\overline{RST}$ signal is also used as a source of power for Tags, Keys and TimeKeys (see respective data sheets). Pin 5 on the 25-Pin D Connector Parallel Printer Port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of Keys, Tags, and TimeKeys. Because the CLK signal provides timing, the relationship between both level and transition from one level to another is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to Keys, Tags, and TimeKeys and a CLK transition is also required to output data. Because signals change state at the same time on the Parallel Printer Port, set up and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will then guarantee that data is valid as the clock changes levels. Pin 17 on the 25-Pin D Connector Parallel Printer Port is called SLCTIN and is used as the data I/O signal for Keys, Tags, and TimeKeys. This is a bi-directional signal. Data is output from this port signal during write cycles, and input from Keys, Tags, and TimeKeys during read cycles. Pin 18 on the 25-Pin D Connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, Tags and TimeKeys, the Parallel Printer Port is being used as a general purpose I/O port. As such, software defines the appropriate commands. In order to avoid having the printer interpret Key, Tag, and TimeKey communications as print commands, the strobe signal (Pin 1 on the D Connector Parallel Printer Port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the Parallel Printer Port signals.

INSTALLATION

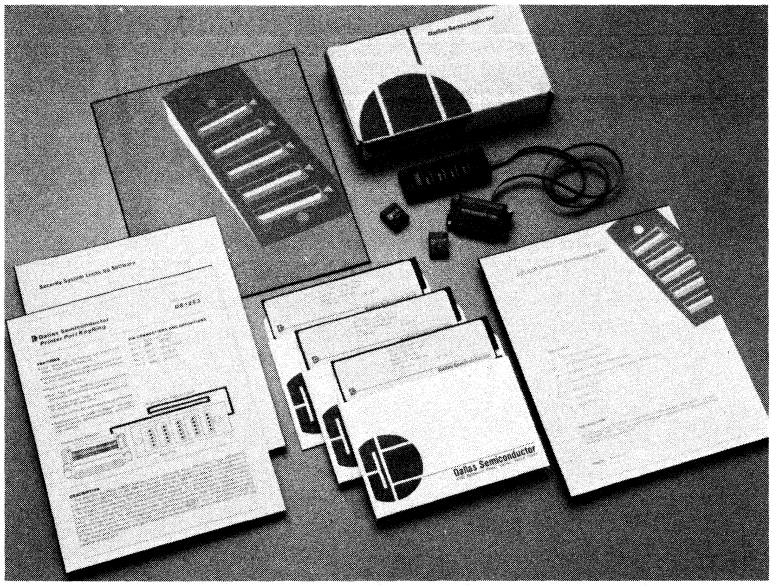
The Parallel Printer Port KeyRing is installed by first removing the printer cable. If the Parallel Printer Port is not used, this step is not necessary. The Parallel Printer Port cable is removed by loosening the top and bottom mounting screws and unplugging the cable. The next step is to install the printer port adapter by loosening the top and bottom mounting screws on the adaptor and plugging the male side of the adapter into the female printer port. The top and bottom screws should then be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the printer port adapter. The top and bottom mounting screws of the printer cable should then be tightened to avoid accidental disconnection. After the printer port adapter has been secured, the key clip can be attached to a convenient spot on the computer cabinet with the supplied adhesive.

SOFTWARE

Upon request Dallas Semiconductor can make available demonstration software with source listing for the IBM PC or IBM PC-compatible computers.

Dallas Semiconductor
Software Authorization Kit

DS1253K



FEATURES

- DS1204S Electronic Key
- DS1201S Electronic Tag
- DS1253 KeyRing with 4-Position Clip
- Demonstration Software for IBM PC on Floppy Disk
- Documentation
- Source Listing
- Data Sheets

INSTRUCTION

Before using the DS1253K, install disk 1 in the default disk drive and type, "TYPE DSC.MEM". This file is the instruction manual which should be read carefully before proceeding.

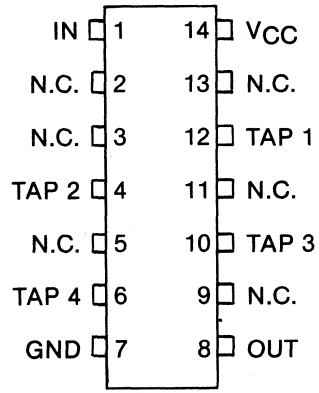
Dallas Semiconductor
Silicon Delay Line

DS1000

FEATURES

- All silicon CMOS time delay
- Delays are stable and precise
- 5 TAPS equally spaced
- TTL compatible
- Standard 14 DIP configuration
- Low profile package
- Delay tolerance ±5%
- Low power CMOS
- Economical
- Auto-insertable

PIN CONNECTIONS



PIN NAMES

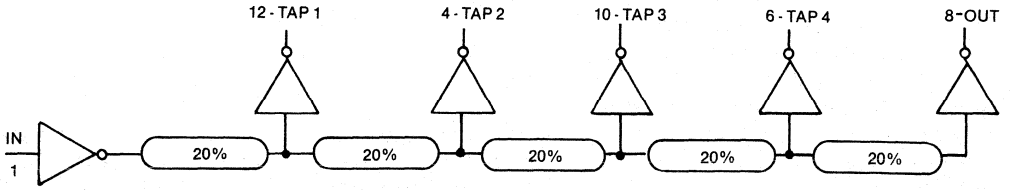
1-4 - Tap Number
OUT - Output
V_{CC} - 5 Volts
GND - Ground
N.C. - No Connection
IN - Input

DESCRIPTION

The DS1000 Series delay lines have five equally spaced taps providing delays from 10 ns to 500 ns. These devices are offered in a standard 14 pin DIP. Since the DS1000 Series is an all-silicon solution, better economy is achieved when compared to the older methods using hybrid techniques. The DS1000 Series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater, with a temperature coefficient of 1500 PPM/°C over the operating temperature range of 0 to 70°C.

The delay line reproduces the input logic level at the output after a fixed delay as specified by the part number. Each output has the capability of driving up to 10 74LS loads. Figure 1 illustrates the logic of the silicon delay line and Table 1 matches part number with the delay time.

LOGIC DIAGRAM Figure 1



PART NO. DELAY TABLE (TPLH, TPHL) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	OUT
DS1000-50	10 ns	20 ns	30 ns	40 ns	50 ns
DS1000-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1000-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1000-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1000-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1000-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1000-250	50 ns	100 ns	150 ns	200 ns	250 ns
DS1000-500	100 ns	200 ns	300 ns	400 ns	500 ns

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −1.0V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to +125°C
Soldering Temperature 260°C for 10 Sec
Short Circuit Output Current 50 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

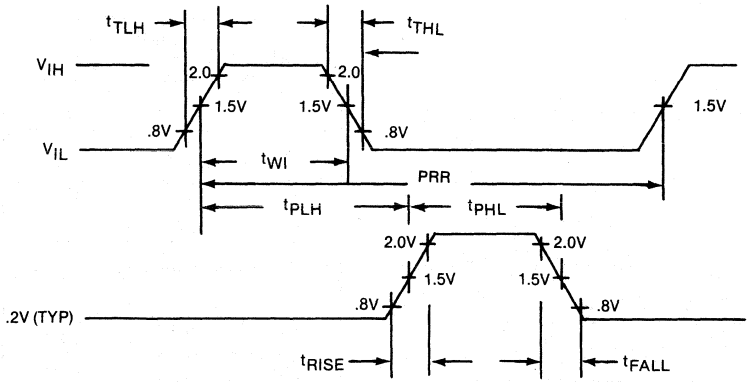
RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Supply		4.75		5.25	V	1
V_{IH} - Logic 1		2.0		V_{CC}	V	1
V_{IL} - Logic 0		−0.5		0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.75 to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			35	mA	2
Input Leakage	I_{IL}			1	uA	
Output @2.4V	I_{OH}	1			mA	
Output @.4V	I_{OL}			−4	mA	

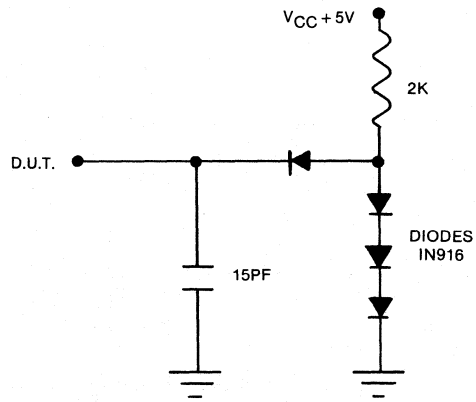
TIMING DIAGRAM—SILICON DELAY LINE



DYNAMIC TEST CONDITIONS

V_{CC} = 5.0 Volts
TA = 25 °C
Load at TAPs per Figure 2
Input Pulse = 0 to 3 Volts
Min. t_{WI} = 40% of total delay
Min. PRR = 4 × t_{WI} minimum
t_{TLH} = 7.0 ns 20-80%
t_{THL} = 7.0 ns 20-80%
t_{PLH} = Table 1
t_{PHL} = Table 1
t_{RISE}, t_{FALL} = 3 n sec. typ.

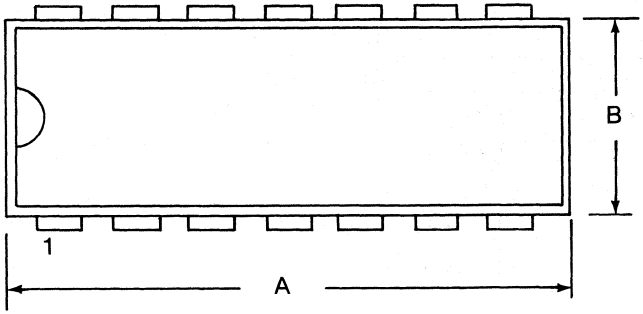
TEST LOAD Figure 2



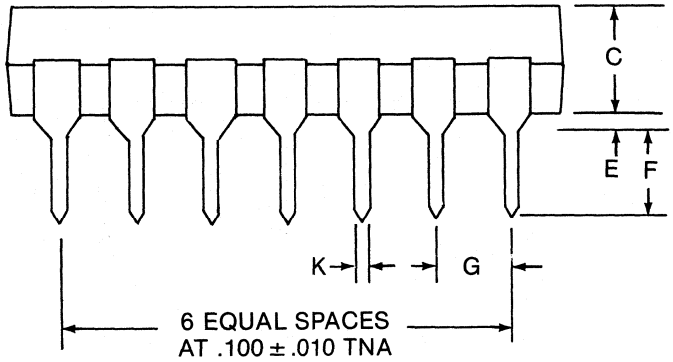
NOTES:

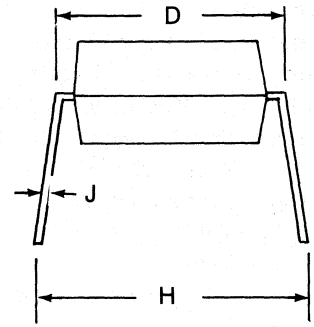
1. All voltages are referenced to ground.
2. Measured with outputs open.

Silicon Delay Line
DS1000



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021





Dallas Semiconductor
DRAM Timer

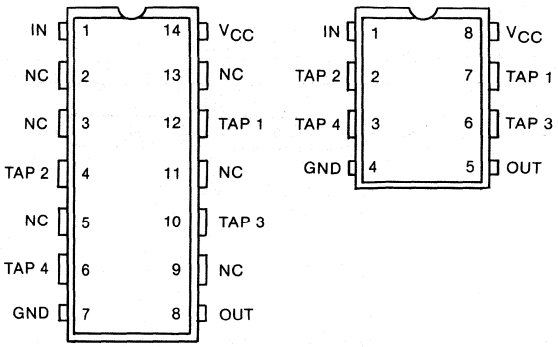
PRELIMINARY

DS1030 14-Pin DIP
DS1031 8-Pin DIP
DS1031S 8-Pin Surface Mount

FEATURES

- All silicon delay line
- Five equally spaced delay outputs
- Leading edge precision
- Tap outputs follow input trailing edge
- TTL-compatible
- DS1030 14-pin DIP replaces hybrid delay lines
- DS1031 space saving 8-pin mini-DIP
- DS1031S surface mount suitable for vapor phase soldering
- Auto insertable
- Low power CMOS
- Economical

PIN CONNECTIONS



PIN NAMES

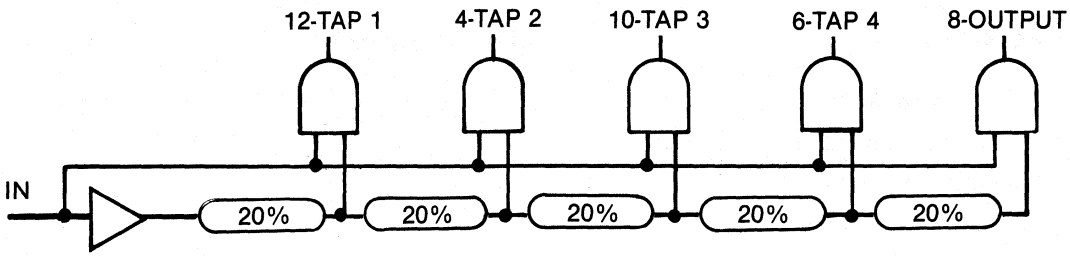
1-4	- Tap Number
OUT	- Output
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1030 series DRAM Timers provide time delays ranging from 20 ns to 500 ns. These devices are available in standard DIP packages. Since the DS1030 series is an all-silicon solution, better economy is achieved when compared to the older methods using hybrid techniques. Internal temperature and voltage compensation circuitry assures accuracy over temperature and voltage extremes.

The DRAM Timer outputs the delayed input leading edge at each tap and at the output as specified by the part number. Input leading edges must be a low to high transition and trailing edges are a high to low transition. All four taps and the output follow the trailing input edge. Each tap and the output has the capability of driving ten 74LS loads. Figure 1 illustrates the logic function of the DRAM Timer; Table 1 matches part number with the delay time.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (TPLH) Table 1

DS1030, DS1031, 1031S	TAP 1	TAP 2	TAP 3	TAP 4	OUTPUT	NOTES
-100	20ns ± 2ns	40ns ± 2ns	60ns ± 3ns	80ns ± 4ns	100ns ± 5ns	3,4,5
-125	25ns ± 2ns	50ns ± 2.5ns	75ns ± 3.75ns	100ns ± 5ns	125ns ± 6.25ns	3,4,5
-150	30ns ± 2ns	60ns ± 3ns	90ns ± 4.5ns	120ns ± 6ns	150ns ± 7.5ns	3,4,5
-175	35ns ± 2ns	70ns ± 3.5ns	105ns ± 5.25ns	140ns ± 7ns	175ns ± 8.75ns	3,4,5
-200	40ns ± 2ns	80ns ± 4ns	120ns ± 6ns	160ns ± 8ns	200ns ± 10ns	3,4,5
-250	50ns ± 2.5ns	100ns ± 5ns	150ns ± 7.5ns	200ns ± 10ns	250ns ± 12.5ns	3,4,5
-500	100ns ± 5ns	200ns ± 10ns	300ns ± 15ns	400ns ± 20ns	500ns ± 25ns	3,4,5

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to 125°C
Soldering Temperature 260°C for 10 Sec
Short Circuit Output Current 50 MA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

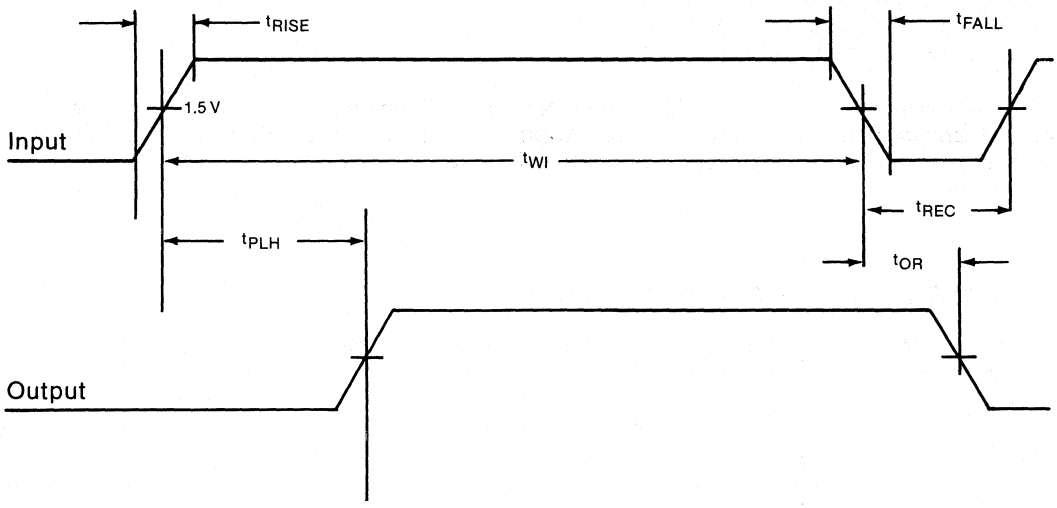
RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{CC}	4.5		5.5	V	1
Logic 1	V_{IH}	2.0		V_{CC}	V	1
Logic 0	V_{IL}	−0.5		0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		20		mA	2
Input Leakage	I_{IL}	−1.0		+1.0	*u*A	
Output @2.4V	I_{OH}	1.0			mA	2
Output @0.4V	I_{OL}			−4.0	mA	2

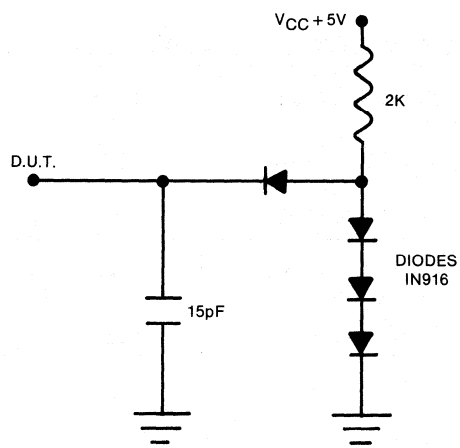
TIMING DIAGRAM Figure 2



DYNAMIC TEST CONDITIONS

V_{CC} = 5.0 Volts
T_A = 25 °C
Load at Tap per Figure 3
Input Pulse = 0 to 3 Volts
t_{WI} Min. = 100% t_{PLH}
t_{PLH} Per Table 1
t_{OR} = 5ns Min. 40ns Max.
t_{REC} = 40ns Min.
t_{RISE}, t_{FALL} = 3ns

TEST LOAD Figure 3

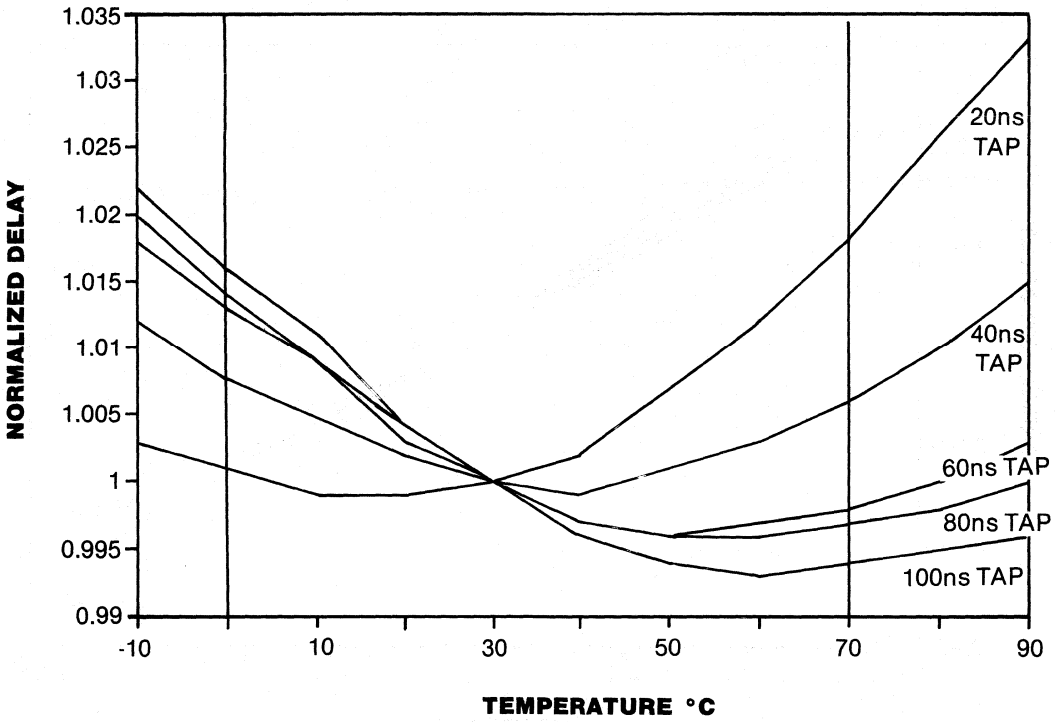


NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. The tolerances specified in Table 1 are measured in accordance with dynamic test conditions.
4. Figure 4 shows typical time delay changes as a function of temperature.
5. Figure 5 shows typical time delay changes as a function of voltage.

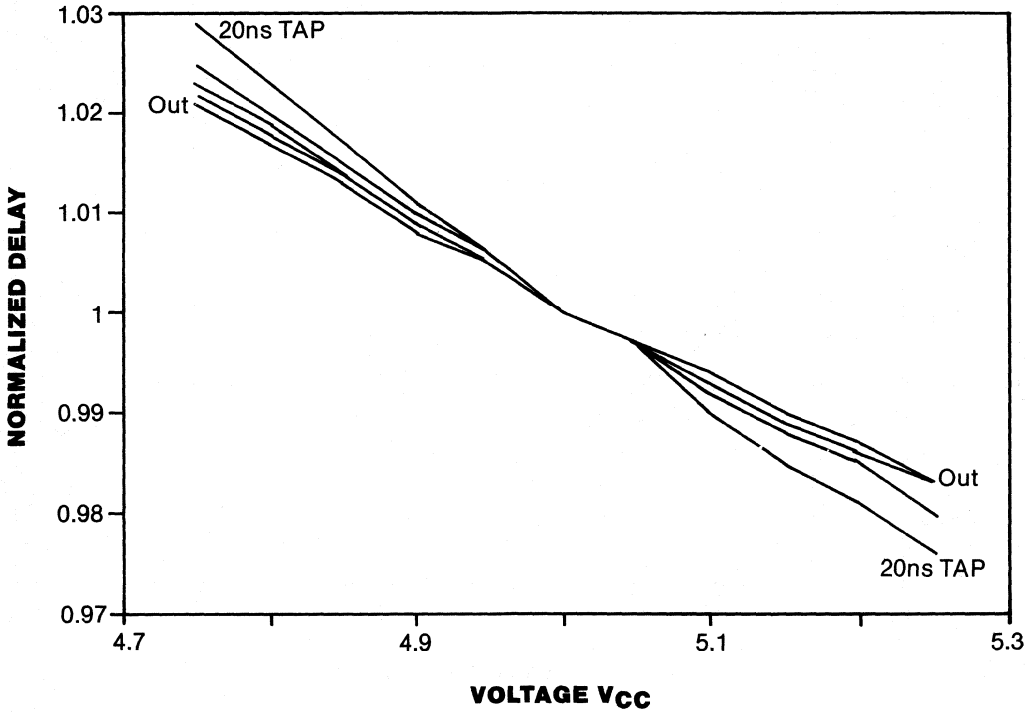
TEMPERATURE VARIATION Figure 3

Typical DS1030-100



NOTE:
Temperature variation shown is for leading edges only; trailing edges follow the input.

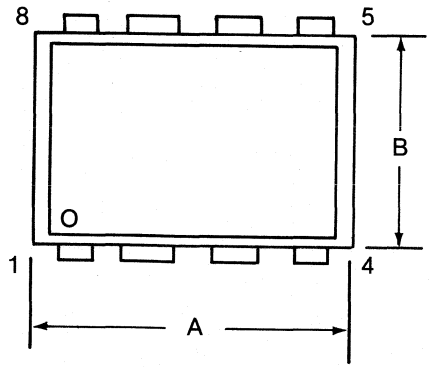
VOLTAGE VARIATION Figure 4
Typical DS1030-100



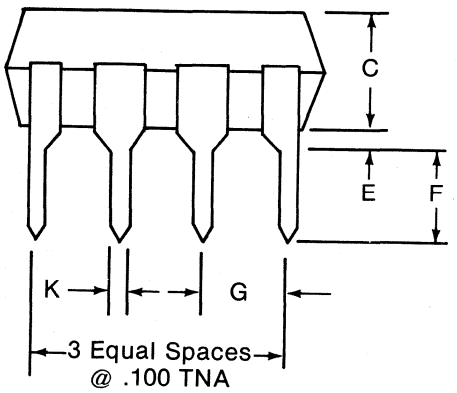
NOTE:
Voltage variation shown is for leading edges only; trailing edges follow the input.

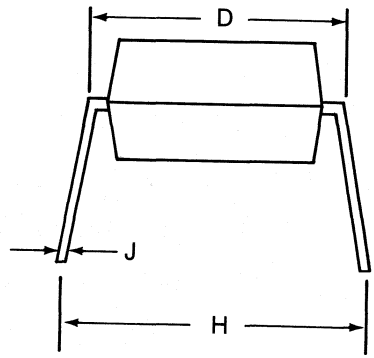
DS1030 and DS1031S DRAM Timer

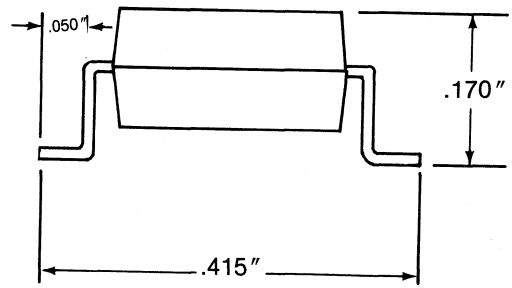
8-PIN DIP AND SURFACE MOUNT



DIM.	INCHES	
	MIN.	MAX.
A	.360	.400
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021

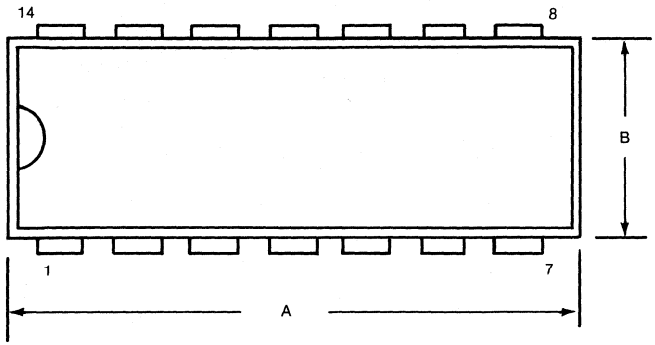




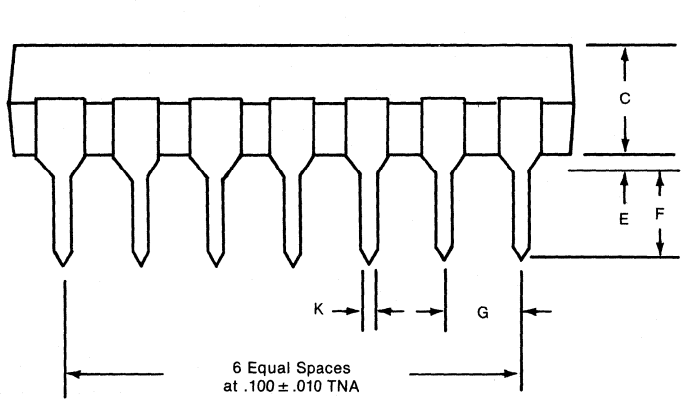


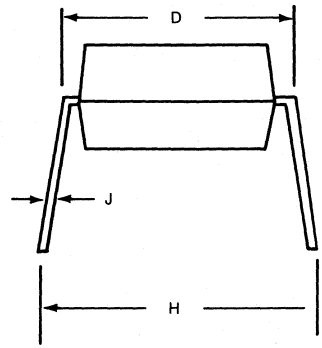
DS1030 DRAM Timer

14-PIN DIP



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021





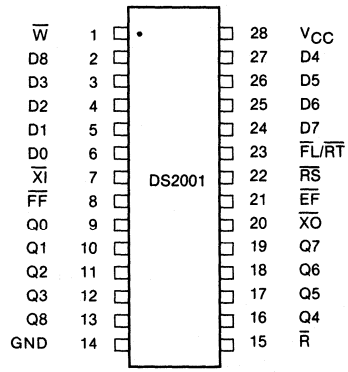
Dallas Semiconductor
2048 x 9 FIFO

PRELIMINARY
DS2001

FEATURES

- First-in, first-out memory based architecture
- Flexible 2048 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Retransmit capability
- High performance
- Available in 120ns and 150ns access times

PIN CONNECTIONS



PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL}/\overline{RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO}$	- Expansion Out
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground

DESCRIPTION

The DS2001 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the DS2001 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register based FIFOs, the DS2001 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the DS2001 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

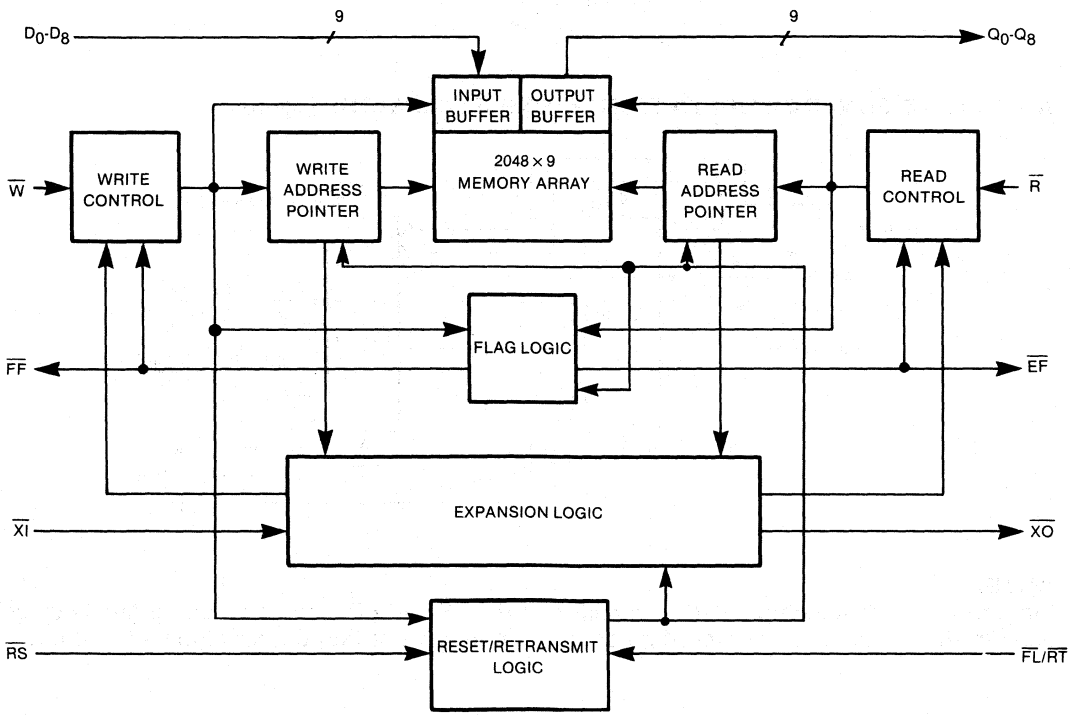
Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 2047. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2001 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2001 allows connecting the read, write, data in, and data out lines of the DS2001 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins, as appropriate (see the Expansion Timing section for a more complete discussion).

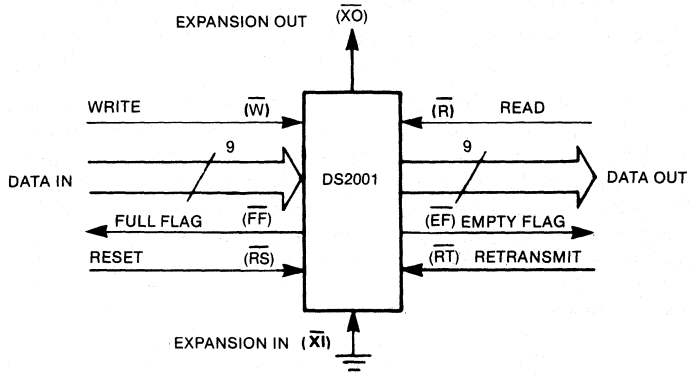
BLOCK DIAGRAM Figure 1



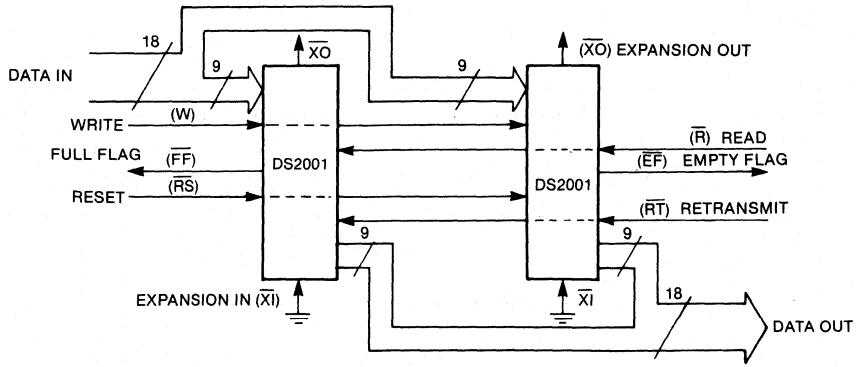
SINGLE DEVICE CONFIGURATION
A single DS2001 may be used when application requirements are for 2048 words or less. The DS2001 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

WIDTH EXPANSION
Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 3 demonstrates an 18-bit word width by using two DS2001s. Any word width can be attained by adding additional DS2001s.

A SINGLE 2048 x 9 FIFO CONFIGURATION Figure 2



A 2048 x 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

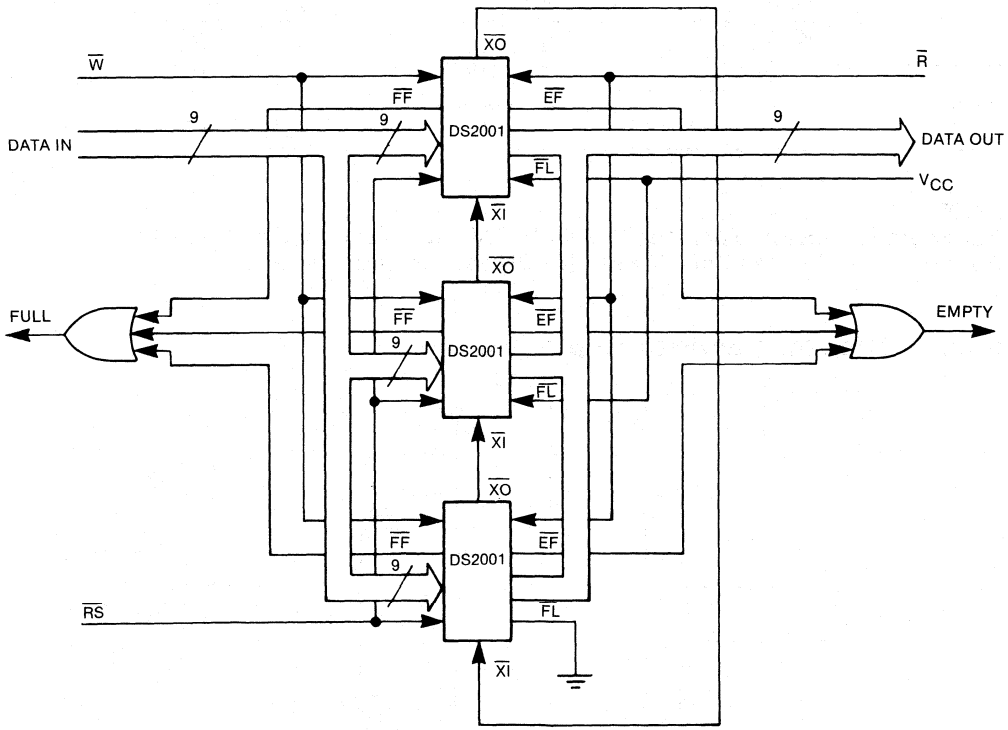
The DS2001 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 4 demonstrates Depth Expansion using three DS2001s. Any depth can be attained by adding additional DS2001s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2001 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.

A 6144 x 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



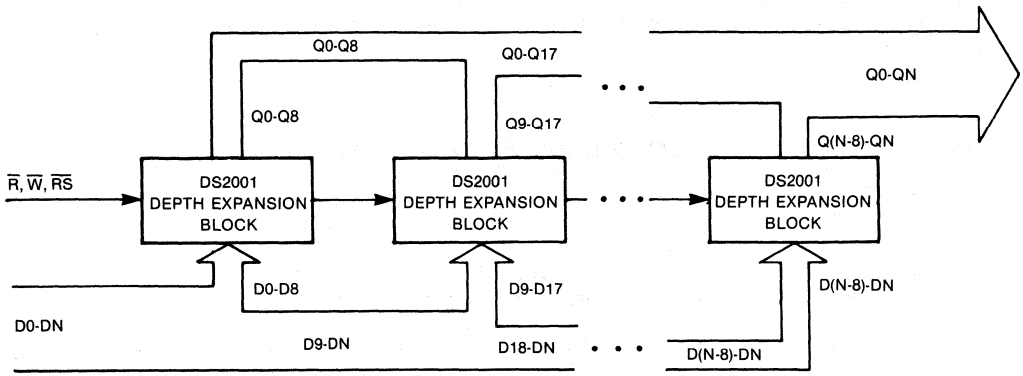
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing DS2001s, as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

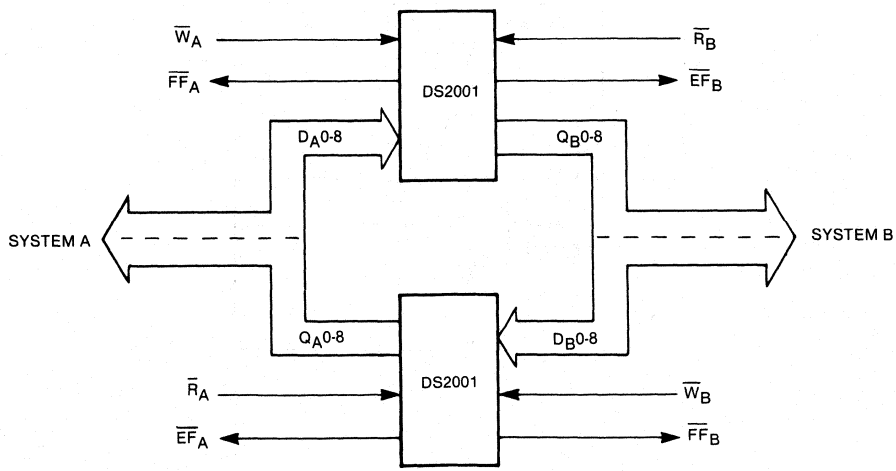
COMPOUND FIFO EXPANSION Figure 5



NOTES:

1. For depth expansion block see DEPTH EXPANSION section and Figure 4.
2. For flag operation see WIDTH EXPANSION section and Figure 3.

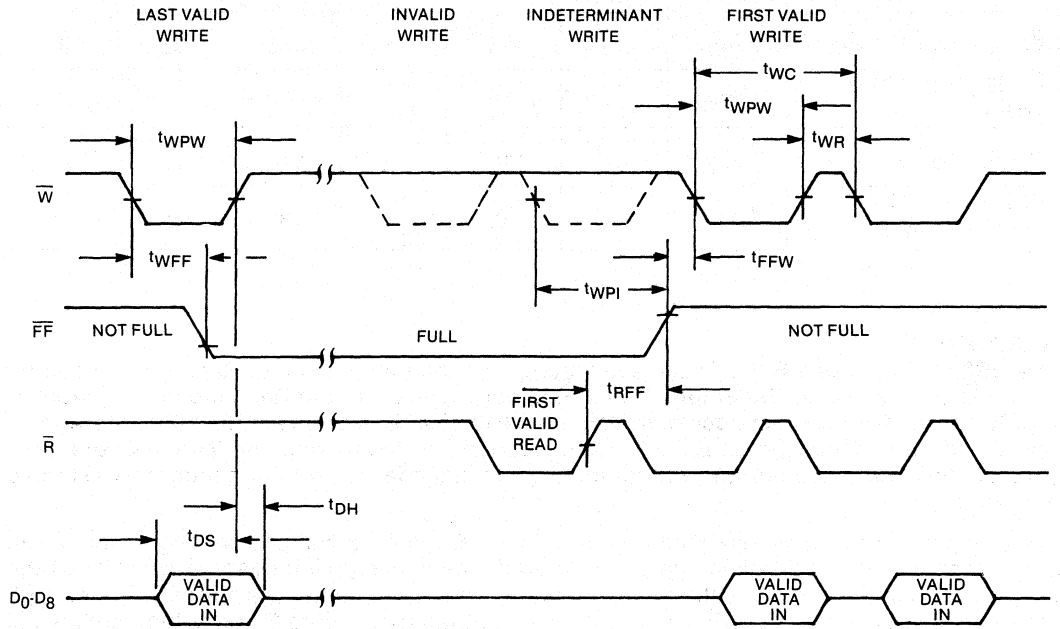
BIDIRECTIONAL FIFO APPLICATION Figure 6



WRITE MODE

The DS2001 initiates a Write Cycle (see Figure 7) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the DS2001 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE A.C. ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC} = 5.0V ± 10%)

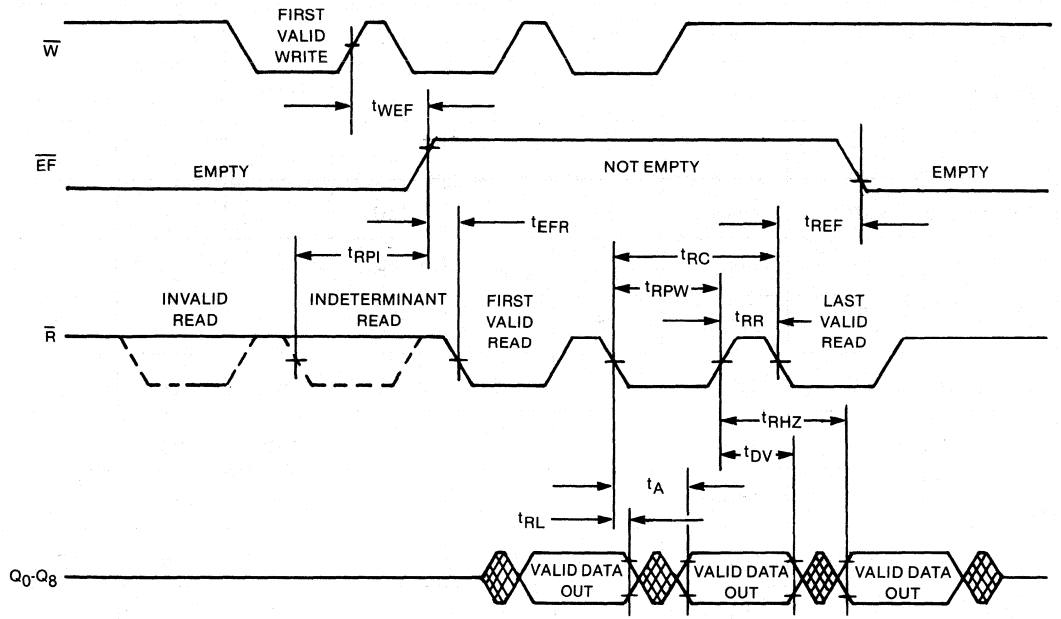
		DS2001-12		DS2001-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Cycle Time	t_{WC}	140		175		ns	
Write Pulse Width	t_{WPW}	120		150		ns	1
Write Recovery Time	t_{WR}	20		25		ns	
Data Set Up Time	t_{DS}	40		50		ns	
Data Hold Time	t_{DH}	10		10		ns	
$\overline{W}$ Low to $\overline{FF}$ Low	t_{WFF}		115		145	ns	2
$\overline{FF}$ High to Valid Write	t_{FFW}		10		10	ns	2
$\overline{R}$ High to $\overline{FF}$ High	t_{RFF}		110		140	ns	2
Write Protect Indeterminant	t_{WPI}		35		35	ns	2

READ MODE

The DS2001 initiates a Read Cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the DS2001 provides a fast access to data from 9 of 18,432 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



READ A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

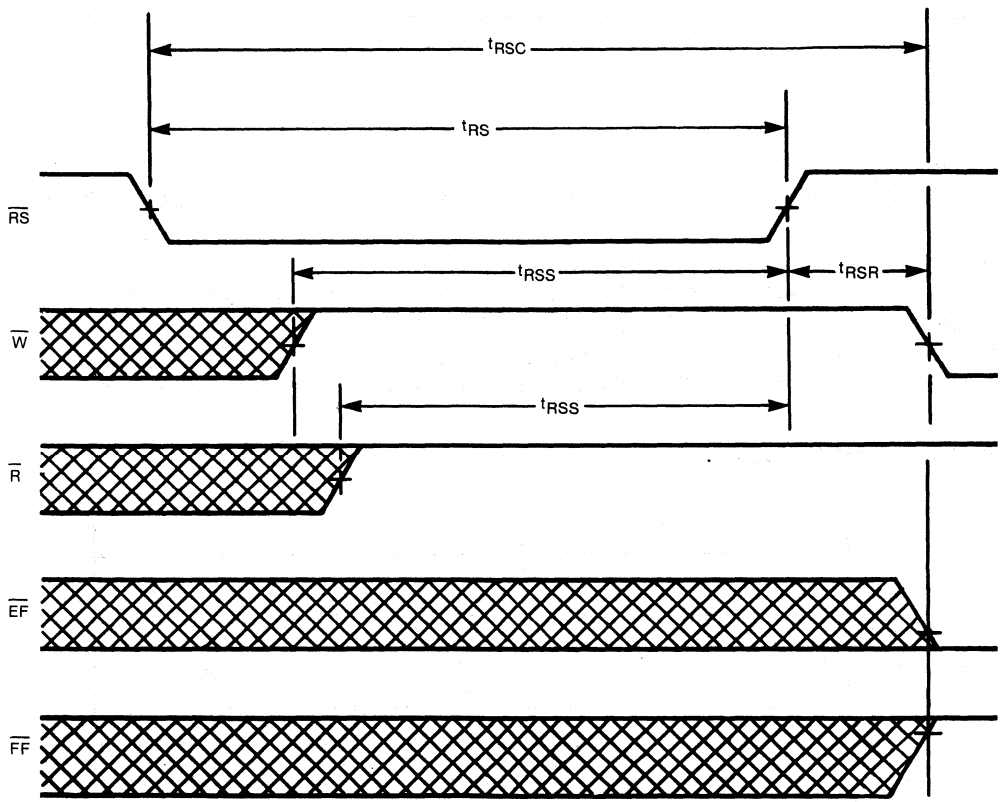
		DS2001-12		DS2001-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	140		175		ns	
Access Time	t_A		120		150	ns	2
Read Recovery Time	t_{RR}	20		25		ns	
Read Pulse Width	t_{RPW}	120		150		ns	1
$\overline{R}$ Low to Low Z	t_{RL}	20		25		ns	2
Data Valid from R High	t_{DV}	5		5		ns	2
$\overline{R}$ High to High Z	t_{RHZ}		35		50	ns	2
$\overline{R}$ Low to EF Low	t_{REF}		115		145	ns	2
$\overline{EF}$ High to Valid Read	t_{EFR}		10		10	ns	2
$\overline{W}$ High to EF High	t_{WEF}		110		140	ns	2
Read Protect Indeterminant	t_{RPI}		35		35	ns	2

RESET

The DS2001 is reset (see Figure 9) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after a power up, before a Write operation can begin.

Although neither $\overline{W}$ nor $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

RESET Figure 9



NOTE:

$\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

RESET A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2001-12		DS2001-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Reset Cycle Time	t_{RSC}	140		175		ns	
Reset Pulse Width	t_{RS}	120		150		ns	1
Reset Recovery Time	t_{RSR}	20		25		ns	
Reset Set Up Time	t_{RSS}	100		130		ns	

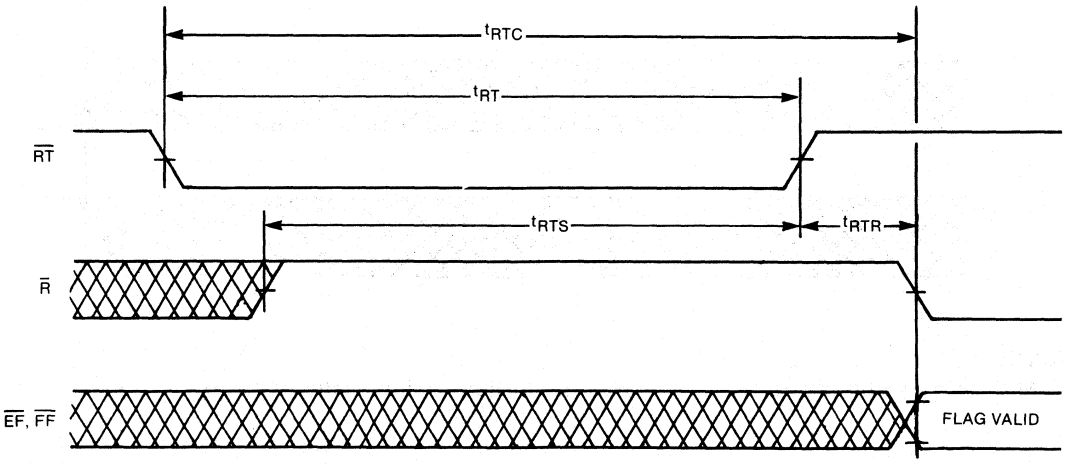
RETRANSMIT

The DS2001 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 10).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

RETRANSMIT Figure 10



RETRANSMIT
A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2001-12		DS2001-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Retransmit Cycle Time	t_{RTC}	140		175		ns	
Retransmit Pulse Width	t_{RT}	120		150		ns	1
Retransmit Recovery Time	t_{RTR}	20		25		ns	
Retransmit Set Up Time	t_{RTS}	100		130		ns	

NOTE:
$\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

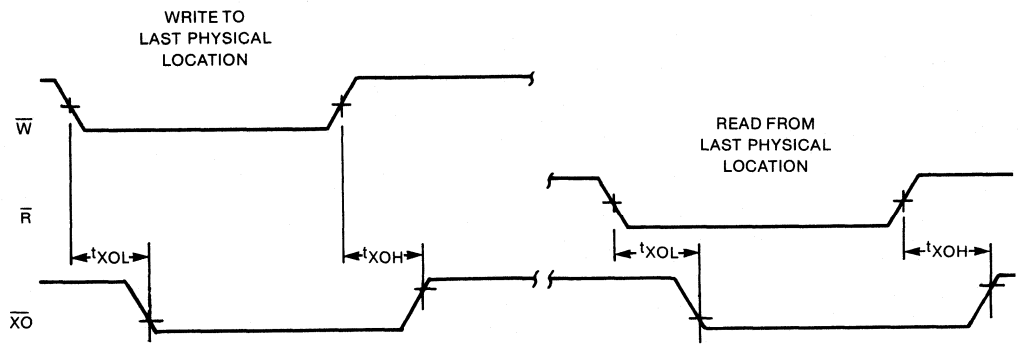
EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given DS2001 will begin writing and reading as soon as valid WRITE and READ signals begin, provided FL was grounded at RESET time. A DS2001 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 11

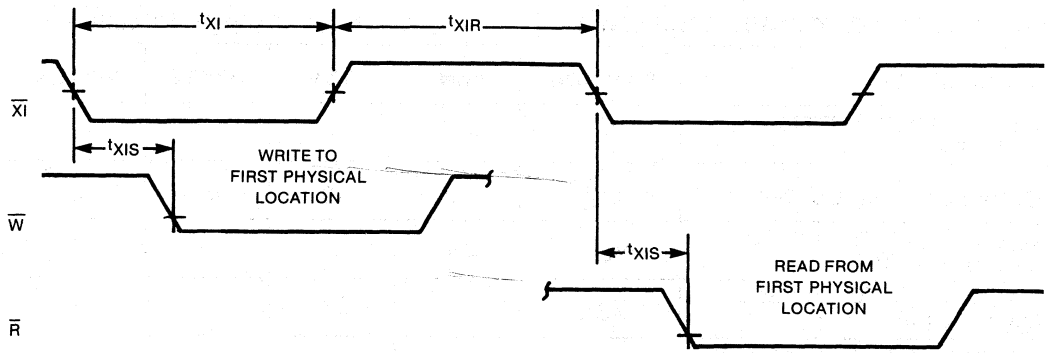


EXPANSION LOGIC
A.C. ELECTRICAL CHARACTERISTICS

(0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2001-12		DS2001-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Out Low	t_{XOL}		90		115	ns	
Expansion Out High	t_{XOH}		100		125	ns	
Expansion In Pulse Width	t_{XI}	115		145		ns	1
Expansion In Recovery Time	t_{XIR}	20		25		ns	
Expansion In Set Up Time	t_{XIS}	50		60		ns	

EXPANSION IN TIMING Figure 12



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin relative to Ground -0.5V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Total Device Power Dissipation 1 Watt
Output Current per Pin 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND	0	0	0	V	
Logic "1" Voltage All Inputs	V_{IH}	2.0		$V_{CC}+0.3$	V	3
Logic "0" Voltage	V_{IL}	−0.3		+0.8	V	3,4

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C) (V_{CC} = 5.0 volts ± 10%)

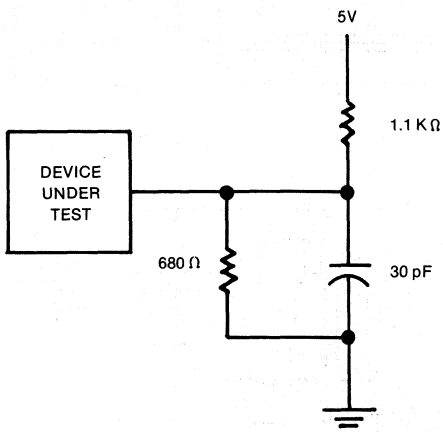
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	−1	1	uA	5
Output Leakage Current	I_{OL}	—10	10	uA	6
Output Logic "1" Voltage I_{OUT} = −1 mA	V_{OH}	2.4		V	3
Output Logic "0" Voltage I_{OUT} = 4 mA	V_{OL}		0.4	V	3
Average V_{CC} Power Supply Current	I_{CC1}		80	mA	7
Average Standby Current ($\overline{R} = \overline{W} = \overline{RST} = \overline{FL/RT} = V_{IH}$)	I_{CC2}		8	mA	7
Power Down Current (All Inputs ≥ V_{CC} − 0.2V)	I_{CC3}		500	uA	7

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	7	pF	
Capacitance on Output Pins	C_Q	12	pF	8

NOTES:
1. Pulse widths les than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to Ground.
4. – 1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \geq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.

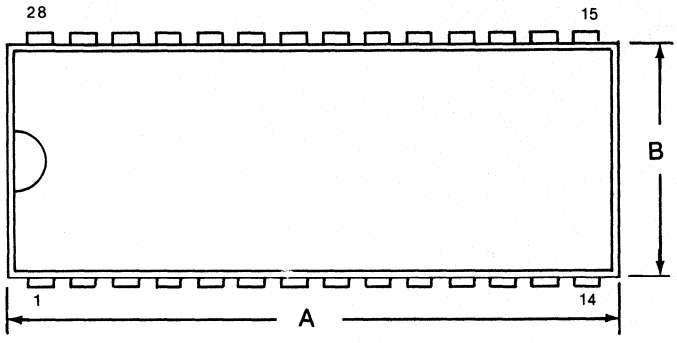
OUTPUT LOAD Figure 13



A.C. TEST CONDITIONS:

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Level	0.8 V and 2.2 V
Ambient Temperature	0 °C to 70 °C
V_{CC}	5.0 V ± 10%

PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS Figure 14



DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

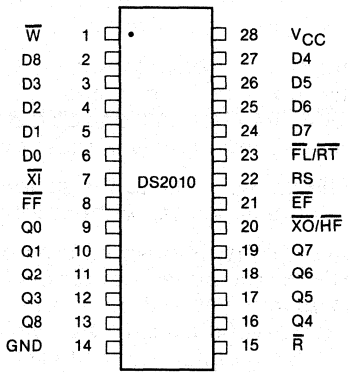
Dallas Semiconductor
1024 x 9 FIFO

PRELIMINARY
DS2010

FEATURES

- First-in, first-out memory based architecture
- Flexible 1024x9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 120ns and 150ns access times

PIN CONNECTIONS



PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL}/\overline{RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO}/\overline{HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground

DESCRIPTION

The DS2010 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the DS2010 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register based FIFOs, the DS2010 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the DS2010 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

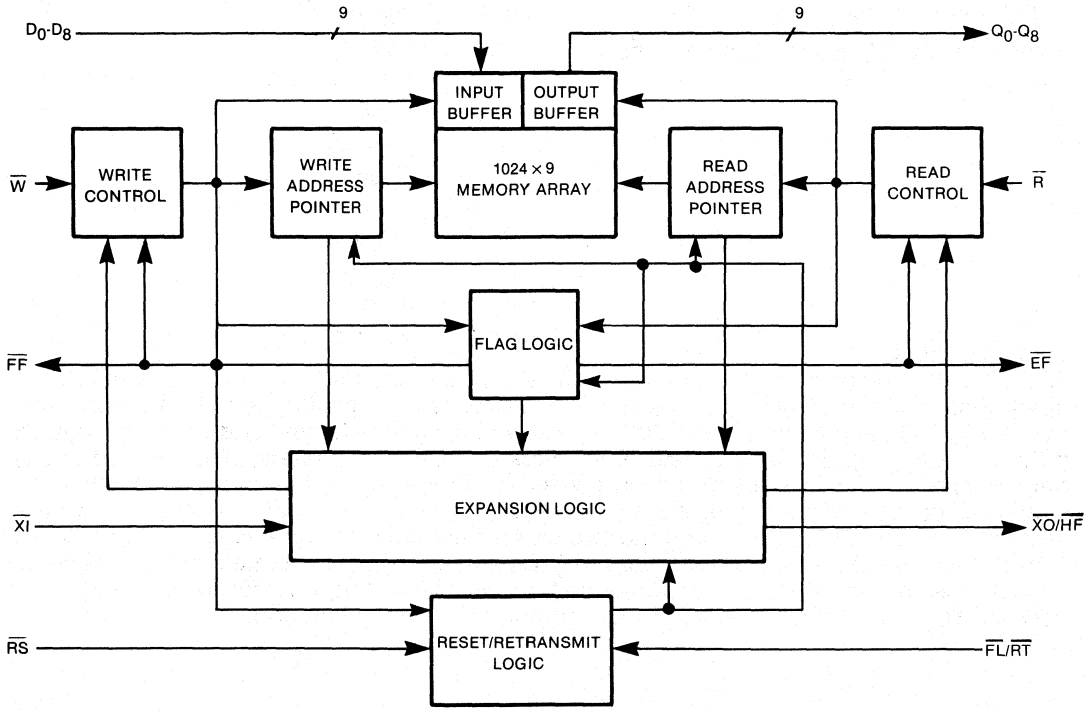
Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 1023. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2010 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2010 allows connecting the read, write, data in, and data out lines of the DS2010 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins, as appropriate (see the Expansion Timing section for a more complete discussion).

BLOCK DIAGRAM Figure 1



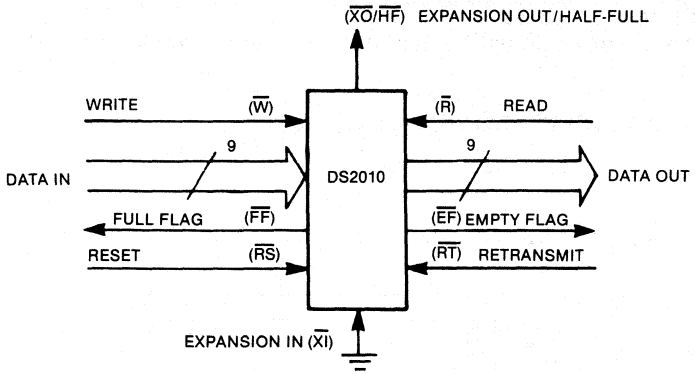
SINGLE DEVICE CONFIGURATION

A single DS2010 may be used when application requirements are for 1024 words or less. The DS2010 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

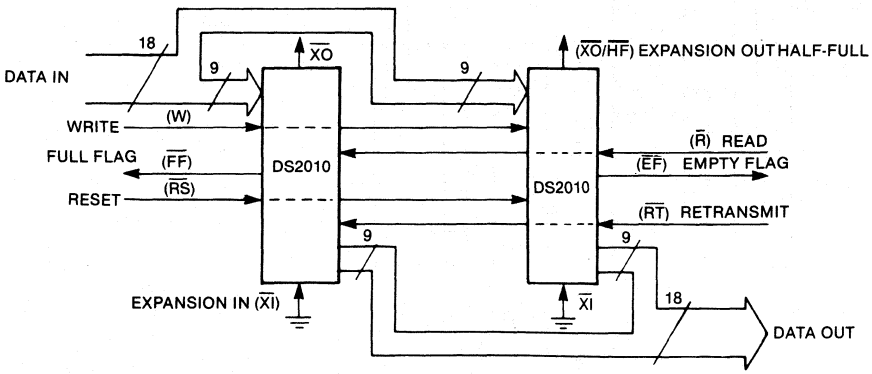
WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 3 demonstrates an 18-bit word width by using two DS2010s. Any word width can be attained by adding additional DS2010s.

A SINGLE 1024 x 9 FIFO CONFIGURATION Figure 2



A 1024 x 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:

Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

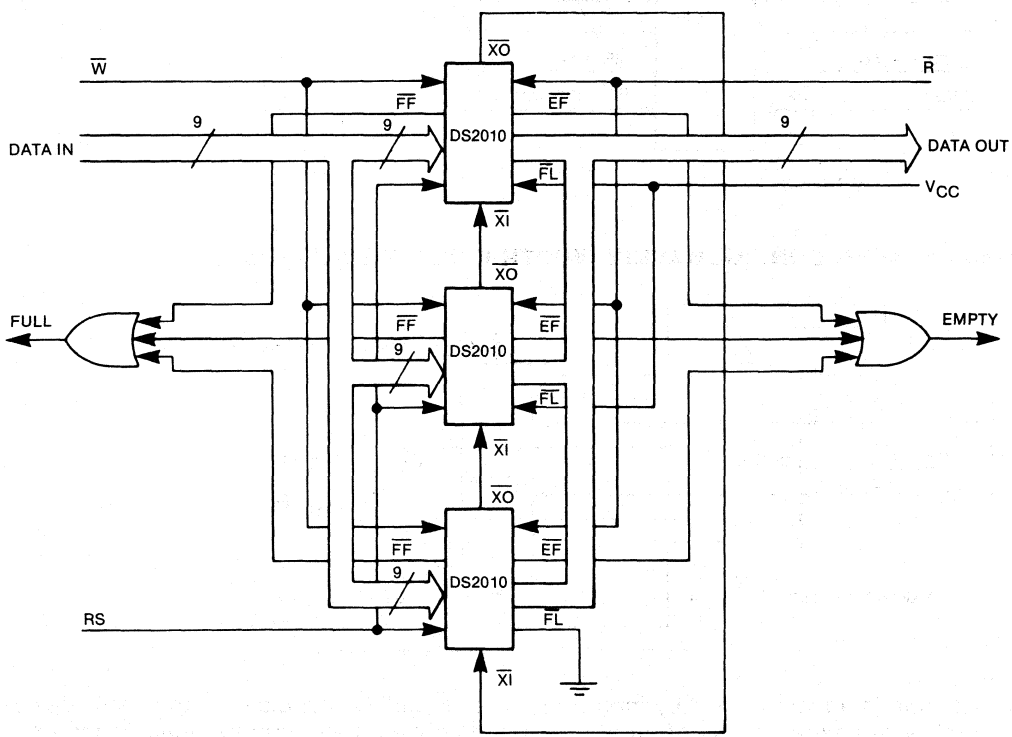
The DS2010 can easily be adapted to applications when the requirements are for greater than 1024 words. Figure 4 demonstrates Depth Expansion using three DS2010s. Any depth can be attained by adding additional DS2010s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2010 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.

A 3072 x 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



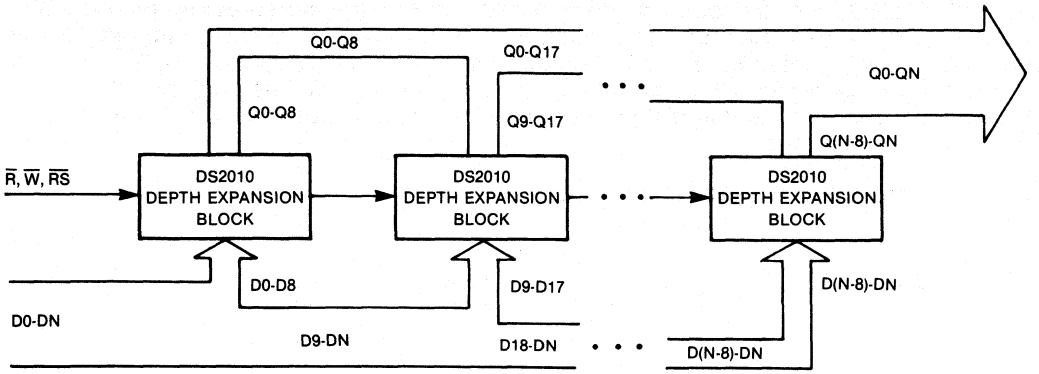
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing DS2010s, as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

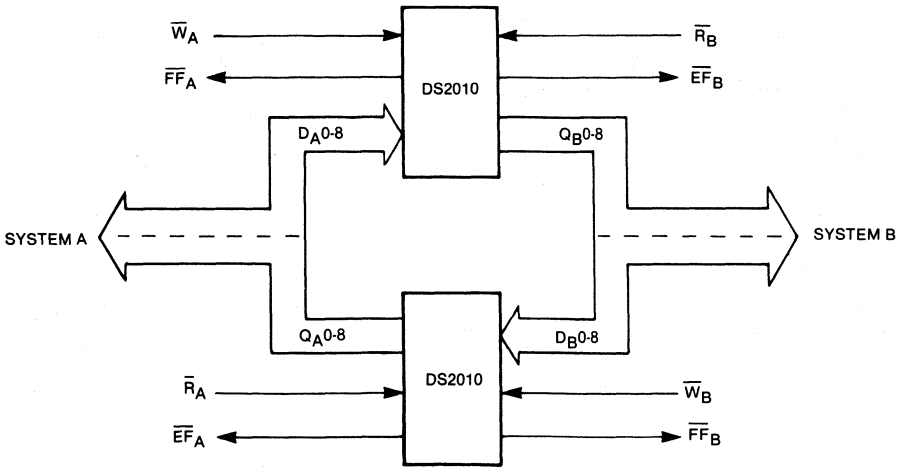
COMPOUND FIFO EXPANSION Figure 5



NOTES:

1. For depth expansion block see DEPTH EXPANSION section and Figure 4.
2. For flag operation see WIDTH EXPANSION section and Figure 3.

BIDIRECTIONAL FIFO APPLICATION Figure 6



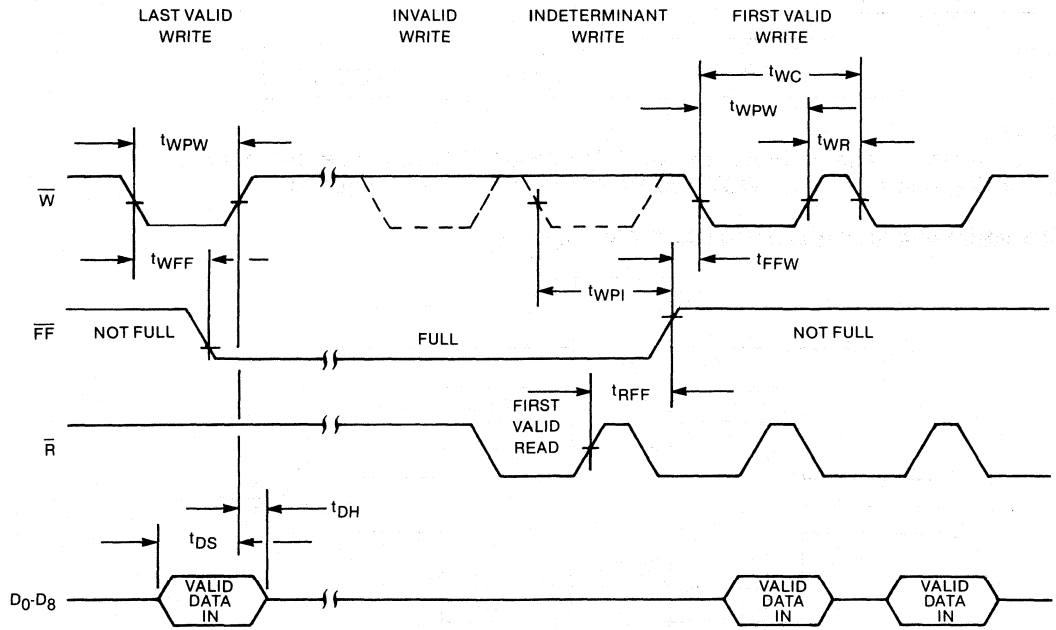
HALF-FULL CAPABILITY

In the single-device and width-expansion modes, the $\overline{XO}/\overline{HF}$ output acts as an indication of a half-full memory. ($\overline{XI}$ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset (forced high) by the rising edge of the read operation.

WRITE MODE

The DS2010 initiates a Write Cycle (see Figure 7) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the DS2010 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

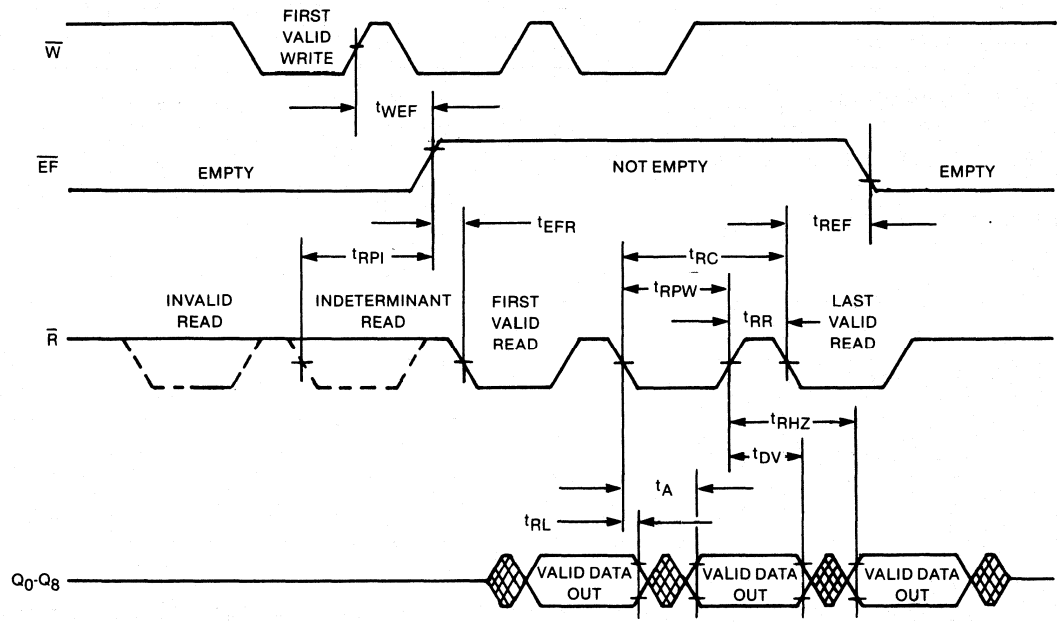
		DS2010-12		DS2010-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Cycle Time	t_{WC}	140		175		ns	
Write Pulse Width	t_{WPW}	120		150		ns	1
Write Recovery Time	t_{WR}	20		25		ns	
Data Set Up Time	t_{DS}	40		50		ns	
Data Hold Time	t_{DH}	10		10		ns	
$\overline{W}$ Low to $\overline{FF}$ Low	t_{WFF}		115		145	ns	2
$\overline{FF}$ High to Valid Write	t_{FFW}		10		10	ns	2
$\overline{R}$ High to $\overline{FF}$ High	t_{RFF}		110		140	ns	2
Write Protect Indeterminant	t_{WPI}		35		35	ns	2

READ MODE

The DS2010 initiates a Read Cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the DS2010 provides a fast access to data from 9 of 9,216 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



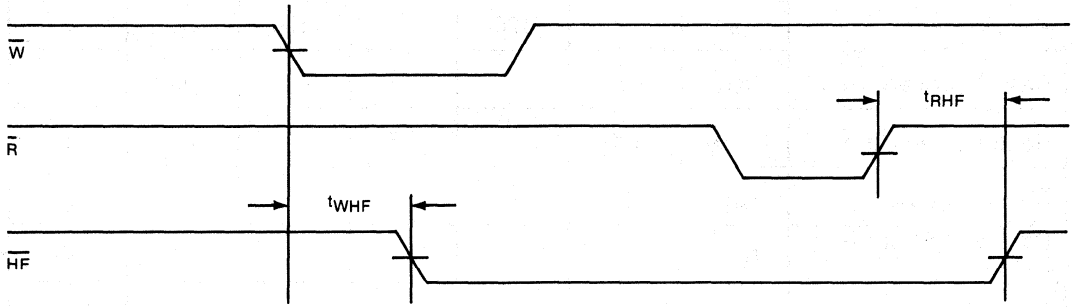
READ A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2010-12		DS2010-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	140		175		ns	
Access Time	t_A		120		150	ns	2
Read Recovery Time	t_{RR}	20		25		ns	
Read Pulse Width	t_{RPW}	120		150		ns	1
$\overline{R}$ Low to Low Z	t_{RL}	20		25		ns	2
Data Valid from R High	t_{DV}	5		5		ns	2
$\overline{R}$ High to High Z	t_{RHZ}		35		50	ns	2
$\overline{R}$ Low to EF Low	t_{REF}		115		145	ns	2
$\overline{EF}$ High to Valid Read	t_{EFR}		10		10	ns	2
$\overline{W}$ High to EF High	t_{WEF}		110		140	ns	2
Read Protect Indeterminant	t_{RPI}		35		35	ns	2

HALF-FULL MODE

Unlike the Full Flag and Empty Flag, the Half-Full Flag does not prevent device reads and writes. The flag is set by the next falling edge of write when the memory is 512 locations full. The flag will remain set until the memory is less than or equal to 512 locations full. The read operation (rising edge), which results in the memory being 512 locations full, removes the flag.

HALF-FULL FLAG TIMING Figure 9



(0°C to +70°C, V_{CC} = 5.0V ± 10%)

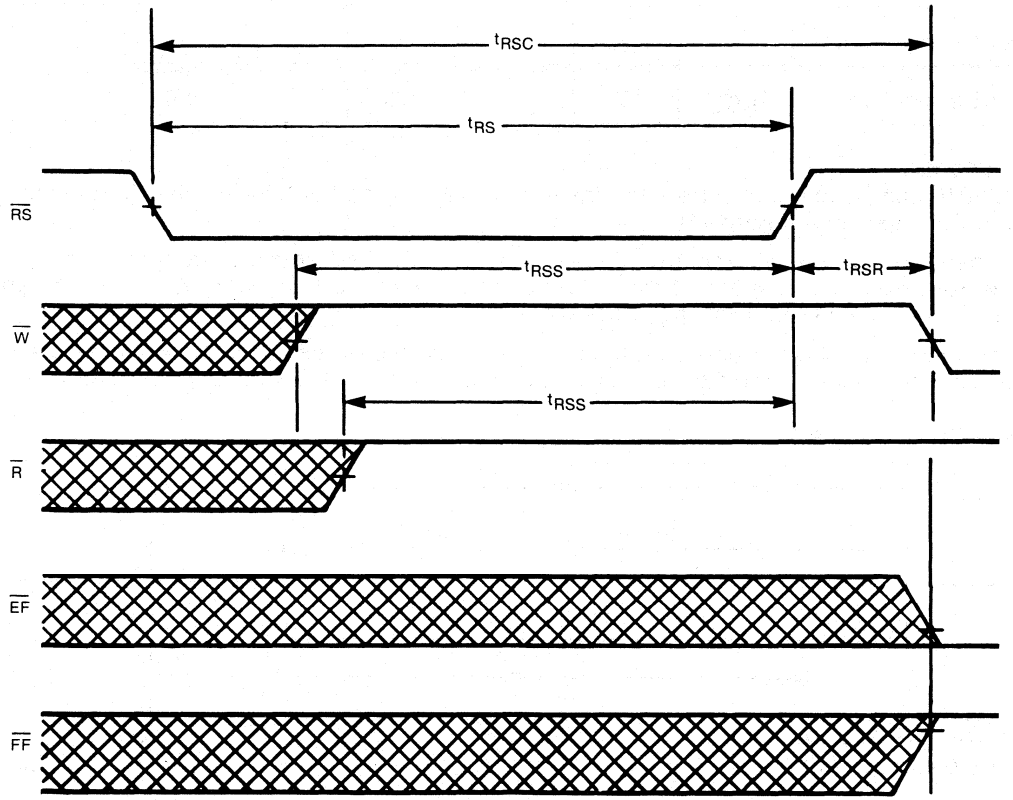
		DS2010-12		DS2010-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Low to Half-Full Flag Low	t_{WHF}		115		145	ns	
Read High to Half-Full Flag High	t_{RHF}		115		145	ns	

RESET

The DS2010 is reset (see Figure 10) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after a power up, before a Write operation can begin.

Although neither $\overline{W}$ nor $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before RS goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

RESET Figure 10



NOTE:
$\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

RESET A.C. ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2010-12		DS2010-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Reset Cycle Time	t_{RSC}	140		175		ns	
Reset Pulse Width	t_{RS}	120		150		ns	1
Reset Recovery Time	t_{RSR}	20		25		ns	
Reset Set Up Time	t_{RSS}	100		130		ns	

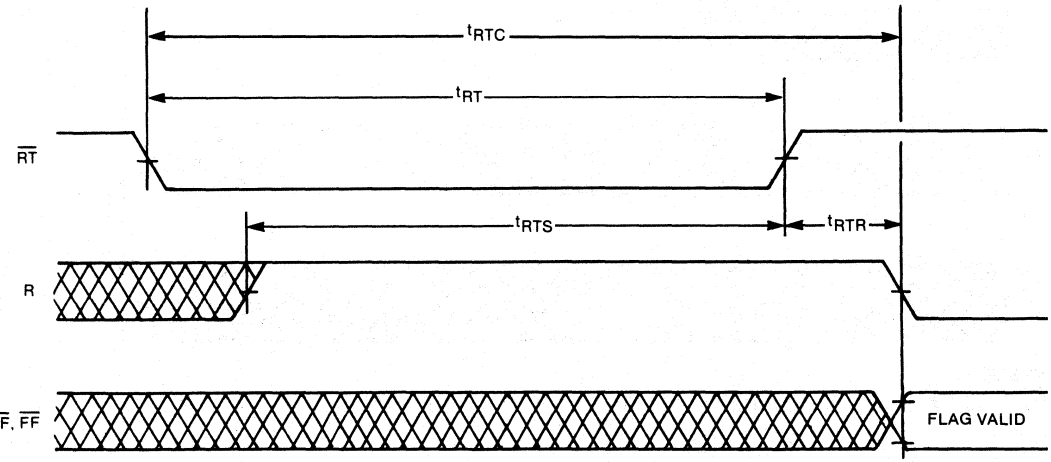
RETRANSMIT

The DS2010 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 11).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 1024 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

RETRANSMIT Figure 11



NOTE:

$\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

RETRANSMIT
A.C. ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2010-12		DS2010-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Retransmit Cycle Time	t_{RTC}	140		175		ns	
Retransmit Pulse Width	t_{RT}	120		150		ns	1
Retransmit Recovery Time	t_{RTR}	20		25		ns	
Retransmit Set Up Time	t_{RTS}	100		130		ns	

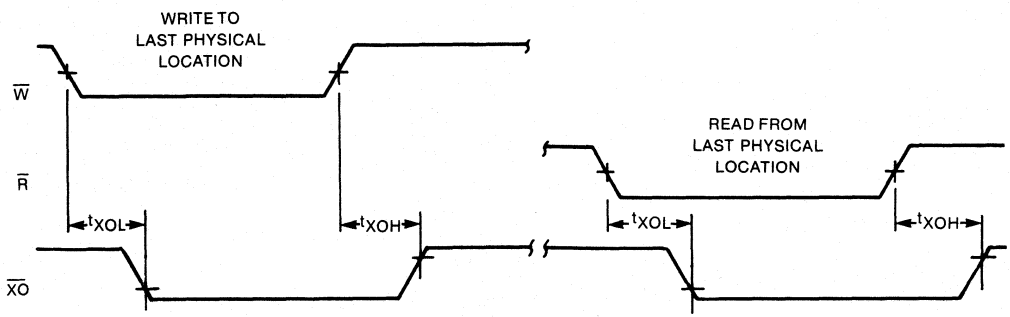
EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

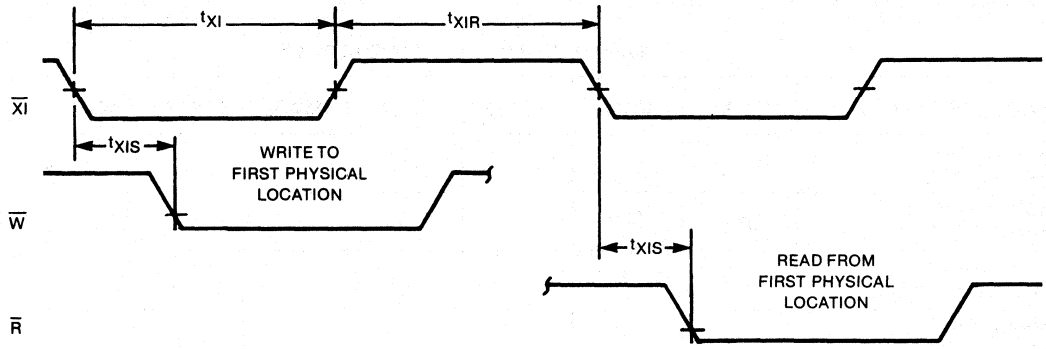
Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given DS2010 will begin writing and reading as soon as valid WRITE and READ signals begin, provided FL was grounded at RESET time. A DS2010 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 12



EXPANSION IN TIMING Figure 13



EXPANSION LOGIC
A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2010-12		DS2010-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Out Low	t_{XOL}		90		115	ns	
Expansion Out High	t_{XOH}		100		125	ns	
Expansion In Pulse Width	t_{XI}	115		145		ns	1
Expansion In Recovery Time	t_{XIR}	20		25		ns	
Expansion In Set Up Time	t_{XIS}	50		60		ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin relative to Ground -0.5V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Total Device Power Dissipation 1 Watt
Output Current per Pin 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND	0	0	0	V	
Logic "1" Voltage All Inputs	V_{IH}	2.0		$V_{CC}+0.3$	V	3
Logic "0" Voltage	V_{IL}	−0.3		+0.8	V	3,4

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C) (V_{CC} = 5.0 volts ± 10%)

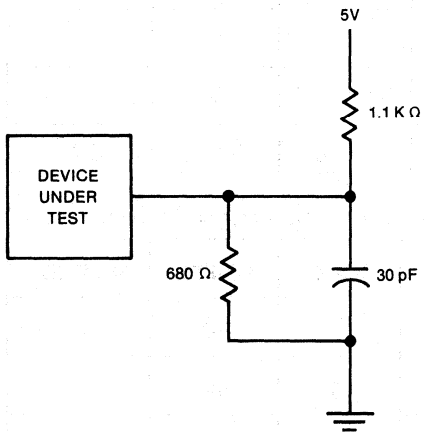
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	−1	1	uA	5
Output Leakage Current	I_{OL}	—10	10	uA	6
Output Logic "1" Voltage I_{OUT} = −1 mA	V_{OH}	2.4		V	3
Output Logic "0" Voltage I_{OUT} = 4 mA	V_{OL}		0.4	V	3
Average V_{CC} Power Supply Current	I_{CC1}		80	mA	7
Average Standby Current ($\overline{R} = \overline{W} = \overline{RST} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{CC2}		8	mA	7
Power Down Current (All Inputs ≥ V_{CC} − 0.2V)	I_{CC3}		500	uA	7

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	7	pF	
Capacitance on Output Pins	C_Q	12	pF	8

NOTES:
1. Pulse widths les than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to Ground.
4. – 1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.

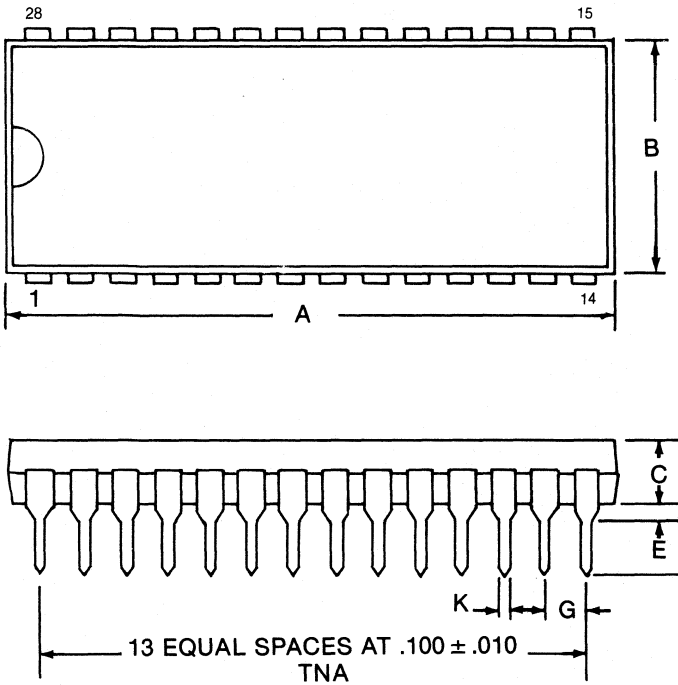
OUTPUT LOAD Figure 14



A.C. TEST CONDITIONS:

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Level	0.8 V and 2.2 V
Ambient Temperature	0 °C to 70 °C
V_{CC}	5.0 V ± 10%

PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS Figure 15

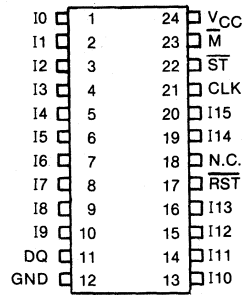


DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

Dallas Semiconductor
Electronic Configurator — *DS1223*

FEATURES
- 16 remote programmable switches
- 9 Bytes of nonvolatile read/write memory
- 16 bit programmable comparator
- 3 pin serial port sets switches and accesses memory
- Greater than 10 years of data retention
- Data and switch settings are automatically protected during power loss
- Full 10% operating range
- Applications include DIP switch replacement; remote P.C. board configuration, mapping, and decoding
- Connects directly to DS1206 Phantom Interface

PIN CONNECTIONS



PIN NAMES

I0-I15	-	Switch, Comparator Input/Outputs
DQ	-	Data Input/Data Output
GND	-	Ground
$\overline{RST}$	-	$\overline{RESET}$
CLK	-	CLOCK
$\overline{ST}$	-	$\overline{STROBE}$
V_{CC}	-	+5 Volts
NC	-	No Connection
$\overline{M}$	-	Comparator Match

DESCRIPTION

The DS1223 Electronic Configurator is a CMOS nonvolatile switch, comparator, and read/write memory circuit designed for personalizing and configurating electronic equipment remotely. The configurator has 16 switches which can be remotely programmed to either Logic 1, Logic 0 or high impedance. Switch pairs can also be connected to simulate 8 SPST switches. In addition, the logic state of 16 inputs can be compared to data contained in nonvolatile memory. There are 16 bytes of nonvolatile read/write memory. Bytes 0, 1, 2, 3, and 4 define switch settings; bytes 5 and 6 relate to the comparator; bytes 7 through 15 are free for any desired use.

A lithium energy source retains information stored in all 16 bytes of memory when power is lost. The electronic configurator monitors V_{CC} for an out of tolerance condition. When such a condition occurs, the lithium energy source is switched on, and write protection is enabled to prevent loss of data. While in the data retention mode the switch/comparator outputs are all in a high impedance mode and all inputs are ignored.

Information is sent to the configurator via a serial input one byte at a time or in a burst where all 16 bytes are either written or read. Interface to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{\text{RESET}}$, Data Input/Output.

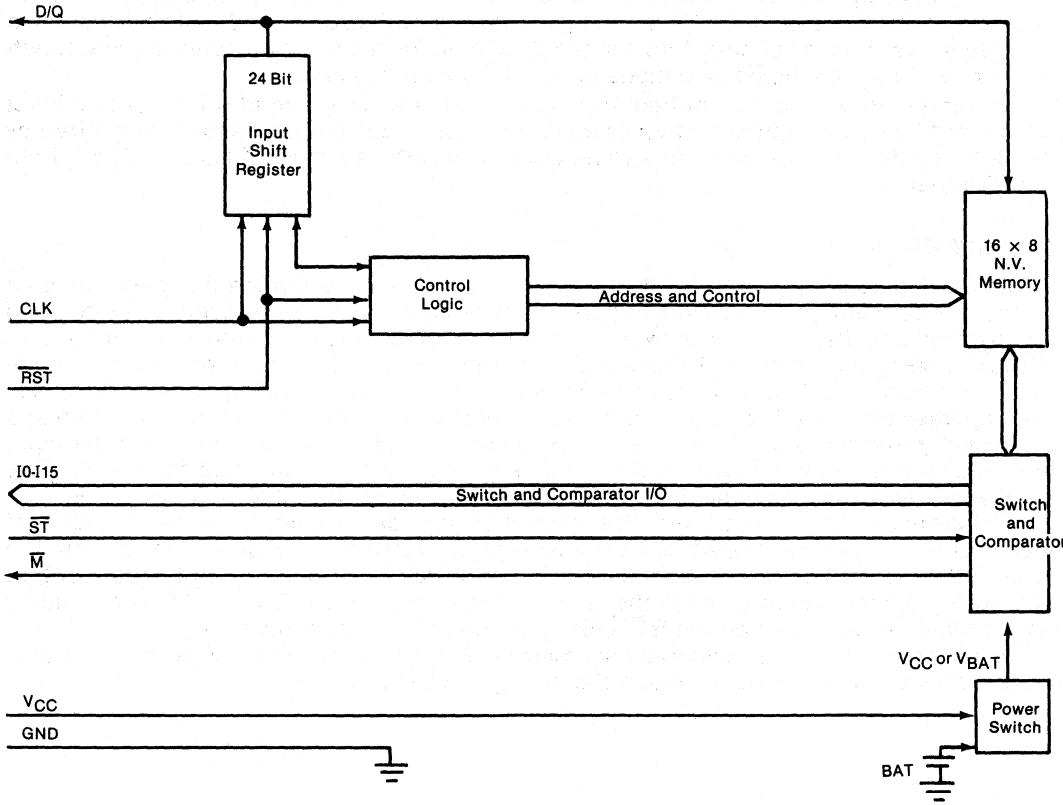
OPERATION

The block diagram (Figure 1) of the electronic configurator illustrates the main elements of the device; namely, input shift register, control logic, nonvolatile memory, switch and comparator circuits, and power switch. To initiate communication with the configurator $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the input shift register providing both address and command information. Each bit is input serially on the rising edge of the clock. Four address bits specify one of 16 nonvolatile memory locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 clocks which load the input shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals 24 plus 8 for byte mode or 24 plus 128 for burst mode.

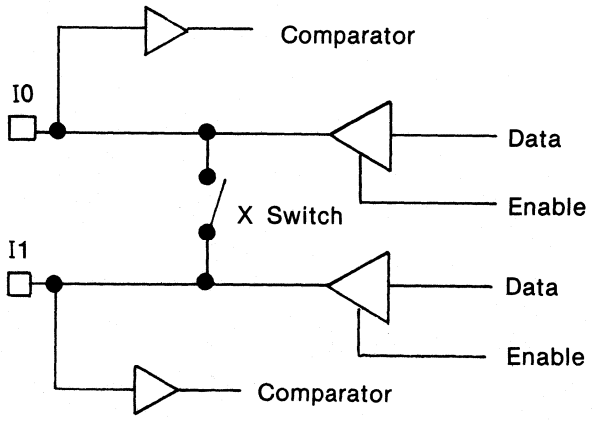
The information stored in the first five bytes of the nonvolatile memory define the status of input/output pins I0-I15. The switch configuration is illustrated in Figure 2. Data stored in nonvolatile memory bytes 6 and 7 contain 16 bits which are compared to the input/output pins I0-I15. When all inputs match the value stored in bytes 6 and 7, the $\overline{\text{MATCH}}$ pin will be latched and driven low when the $\overline{\text{STROBE}}$ input transitions from low to high.

The nine remaining bytes serve as user read/write nonvolatile memory. Figure 3 illustrates the configurator register address and the definition of each bit.

ELECTRONIC CONFIGURATOR BLOCK DIAGRAM Figure 1



CONFIGURATOR SWITCHES Figure 2



X Switch Resistance ≤ 500 Ω

Switch Pairs		
	I0 - I1	I8 - I9
	I2 - I3	I10 - I11
	I4 - I5	I12 - I13
	I6 - I7	I14 - I15

CONFIGURATOR MEMORY ADDRESSES Figure 3

	MSB 7	6	5	4	3	2	1	0 LSB	
Byte 0	I15,I14	I13,I12	I11,I10	I9,I8	I7,I6	I5,I4	I3,I2	I1,I0	X Switch 1 = Closed 0 = Open
Byte 1	I7	I6	I5	I4	I3	I2	I1	I0	Data Out 1 = Logic High 0 = Logic Low
Byte 2	I15	I14	I13	I12	I11	I10	I9	I8	Data Out 1 = Logic High 0 = Logic Low
Byte 3	I7	I6	I5	I4	I3	I2	I1	I0	Enable Out 0 = HIZ
Byte 4	I15	I14	I13	I12	I11	I10	I9	I8	Enable Out 0 = HIZ
Byte 5	I7	I6	I5	I4	I3	I2	I1	I0	Comparison
Byte 6	I15	I14	I13	I12	I11	I10	I9	I8	Comparison
Byte 7									User Byte
Byte 8									User Byte
Byte 9									User Byte
Byte 10									User Byte
Byte 11									User Byte
Byte 12									User Byte
Byte 13									User Byte
Byte 14									User Byte
Byte 15									User Byte

ADDRESS/COMMAND

Each data transfer consists of a three byte address/command input called the address/command. The address/command is shown in Figure 4. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address command fails to meet the exact pattern of read or write the cycle is aborted and all future inputs to the configurator are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The 8 bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address A0 in bit 0, A1 in bit 1, A2 in bit 2, A3 in bit 3. Bits 4 through 7 of the second byte of the address/command must be set at logical 0. If bits 4 through 7 do not equal logical 0, the cycle is aborted and all future inputs to the configurator are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The third byte of the address/command must have a logic 0 in bit 0 through bit 5 and a logical 1 written in bit 6. Bit 7 of byte three of the address/command is used along with bits A0 through A3 in byte 2 to define the burst mode. When A0 through A3 of byte two equals logical 0 and bit 7 of byte three equals logical 1, the configurator will enter the burst mode after the 24 bit address/command sequence is complete.

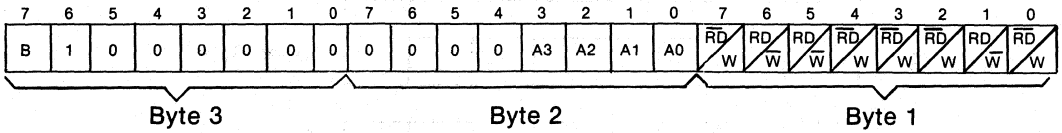
BURST MODE

Burst mode is specified for the electronic configurator when all address bits (A0-A3) of the address/command are set to logical 0 and bit 7 of byte three to logical 1. The burst mode causes 16 consecutive bytes to be read or written. Burst mode terminates when the $\overline{\text{RESET}}$ input is driven low.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{\text{RESET}}$ input high. The input also provides a method of terminating either single byte or multiple byte transfers. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of clock cycles. Address/command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates and D/Q pin goes to a high impedance state if the $\overline{\text{RESET}}$ input is low. The $\overline{\text{RST}}$ input is used only in control of communications with the configurator and has no effect on the nonvolatile memory data. Data transfer is illustrated in Figure 5.

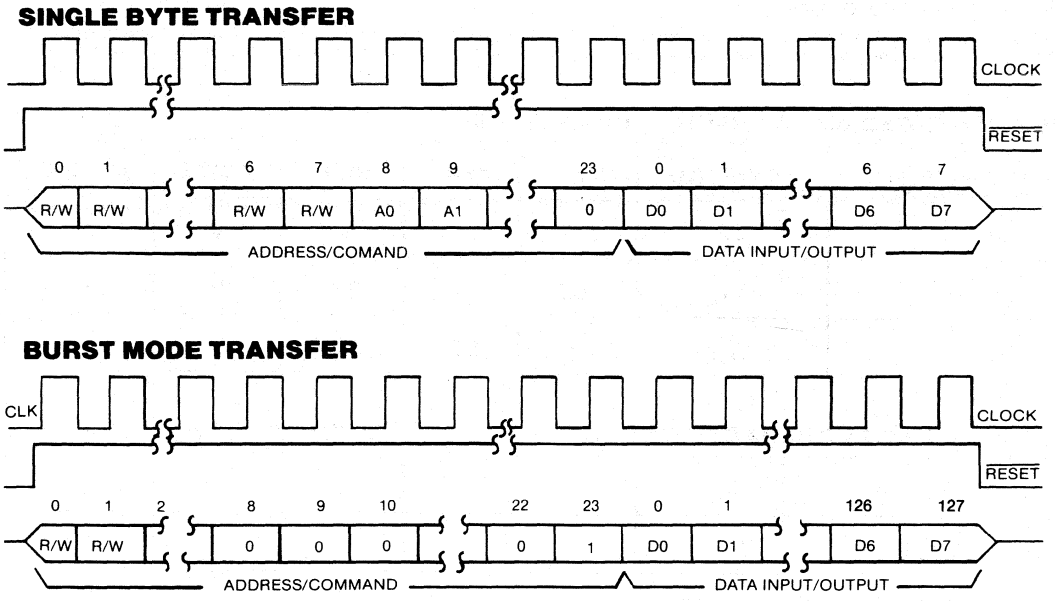
CONFIGURATOR — ADDRESS COMMAND WORD Figure 4



B - Burst
RD - Read
W - Write
A0-A3 - Address

DATA TRANSFER

Figure 5



NOTES
1.) DATA INPUT SAMPLED ON RISING EDGE OF CLOCK
2.) DATA OUTPUT CHANGES ON FALLING EDGE OF CLOCK

DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1 bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

DATA OUTPUT

Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for data output byte 1 bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to 70°C
STORAGE TEMPERATURE	—	−40°C to 70°C
SOLDERING TEMPERATURE	—	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} +.3	V	1
Logic 0	V_{IL}	−0.3		0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C V_{CC} = 5V ±10%)

Input Leakage	I_{IL}			1	uA	5
Output Leakage	I_{LO}			1	uA	5
Output Current @2.4V	I_{OH}	−1			mA	11
Output Current @ .4V	I_{OL}			+4	mA	11
Output Current @2.4V	I_{OH}	−400			uA	12
Output Current @ .4V	I_{OL}			1.6	mA	12
X Switch Impedance	X			500	Ω	7
Active Current	I_{CC1}			10	mA	8
Standby Current	I_{CC2}			2	mA	8, 2

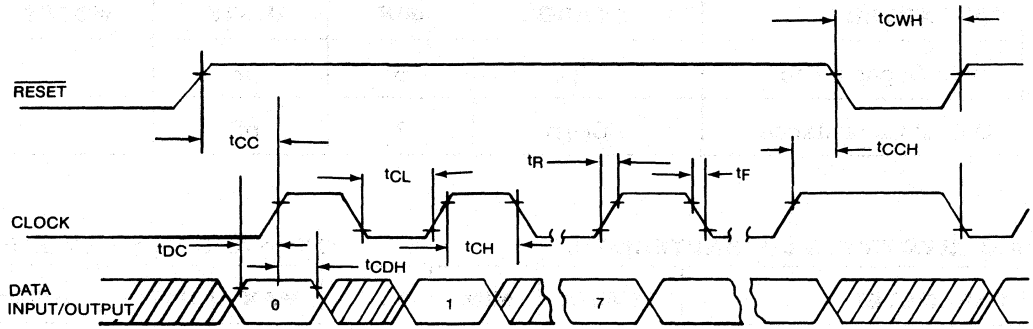
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

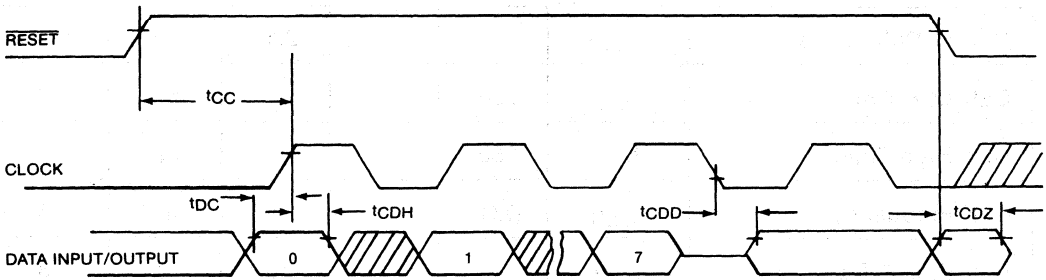
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	3
Data to CLK Hold	t_{CDH}	50			ns	3
CLK to Data Delay	t_{CDD}			200	ns	3, 4, 6
CLK Low Time	t_{CL}	250			ns	3
CLK High Time	t_{CH}	250			ns	3
CLK Frequency	f_{CLK}	D.C.		2.0	MHZ	3
CLK Rise & Fall	t_R, t_F			10	ns	3
$\overline{RST}$ to CLK Set Up	t_{CC}	1			us	3, 9
CLK to $\overline{RST}$ Hold	t_{CCH}	50			ns	3
$\overline{RST}$ Inactive Time	t_{CWH}	1			us	3
$\overline{RST}$ to //O High Z	t_{CDZ}			75	ns	3
Strobe to $\overline{MATCH}$ Valid	t_{SM}			35	ns	3
Input Set-Up	t_{SU}	40			ns	3,4
Input Hold	t_{HD}	10			ns	3,4

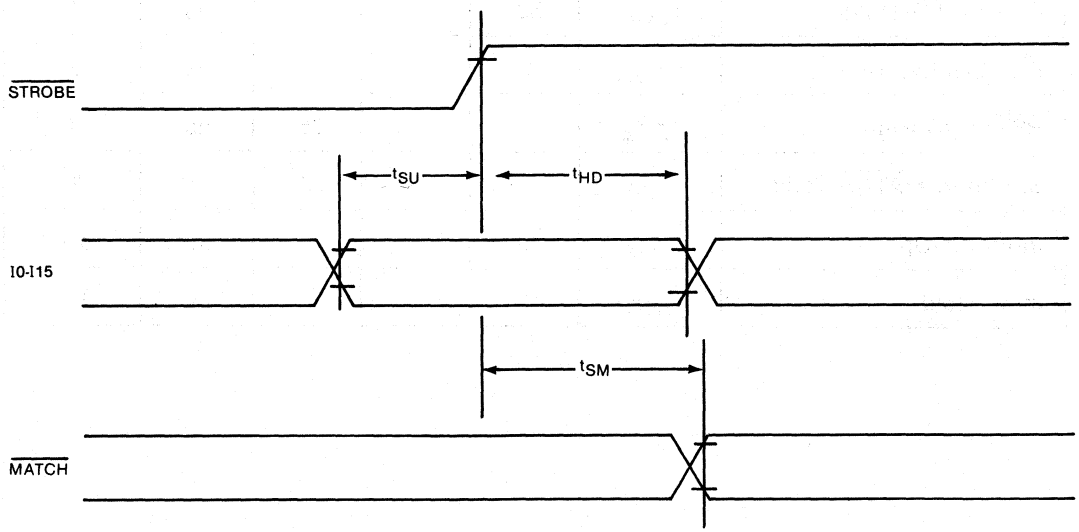
TIMING DIAGRAM—WRITE DATA TRANSFER[10]



TIMING DIAGRAM—WRITE DATA TRANSFER[10]



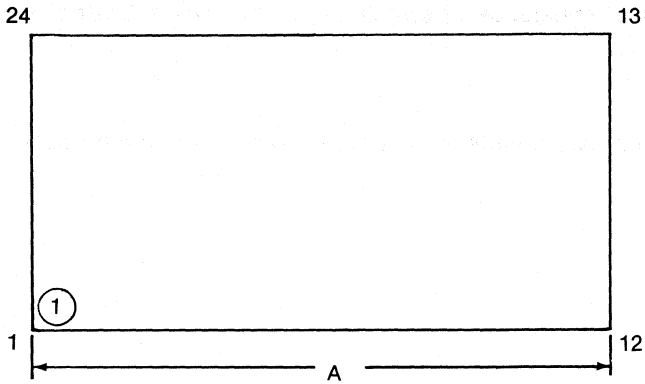
TIMING DIAGRAM—COMPARATOR[10]



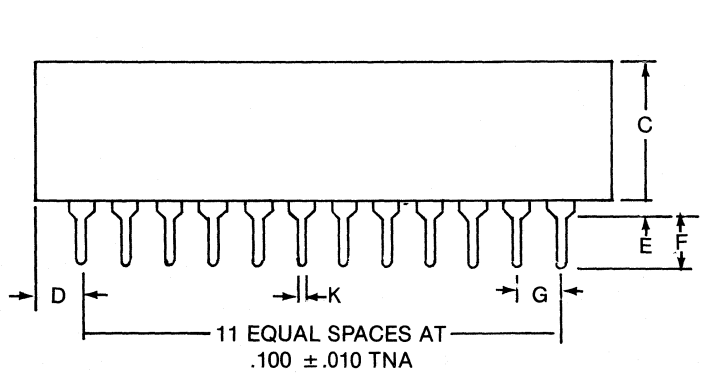
NOTES

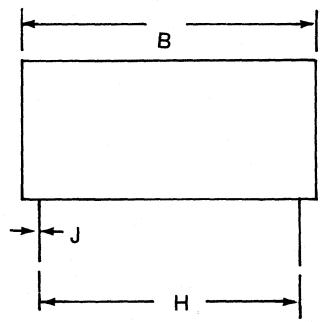
1. All voltages are referenced to GND.
2. $\overline{\text{RESET}}$ = V_{IH}.
3. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
4. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
5. V_{CC} = +5 Volts with outputs open.
6. Load capacitance = 100 pF.
7. X Switch Impedance is the terminal resistance of switch pairs when the X Switch is closed—see Figure 2.
8. Measured with outputs open.
9. Measured at V_{IN} of $\overline{\text{RST}}$ = 3.8V.
10. A period of 100 ns must elapse after data transfer before switches and comparator outputs are valid.
11. Applies to DQ and $\overline{\text{MATCH}}$.
12. Applies to switches.

DS1223
Electronic Configurator



DIM.	INCHES	
	MIN.	MAX.
A	1.320	1.335
B	.670	.685
C	.310	.325
D	.100	.120
E	.025	.035
F	.110	.130
G	.090	.110
H	.600	.650
J	.008	.012
K	.015	.021



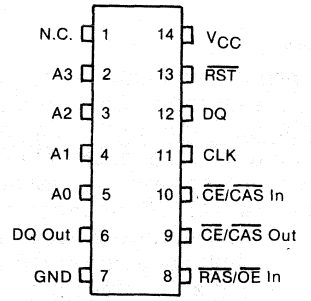


NOTE: Pin 18 is missing by design.

Dallas Semiconductor
Phantom Interface — DS1206

FEATURES
- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory wave forms into a three wire serial port
- Operation is transparent to memory
- Software generated memory cycles activate serial port and transfer data
- High band width—1bit data transfer per 2 memory cycles
- Intercepts memory signals so that pass through connections can be maintained to memory
- Controls communications for as many as ten DS1201 Tags, DS1204 Keys or DS1290 Eliminators
- Low power CMOS circuitry

PIN CONNECTIONS



PIN NAMES

Pin 1	- N.C.	No connection
Pins 2,3, 4,5	- A0-A3	Memory address bus
Pin 6	- DQ Out	Data out to memory bus
Pin 7	- GND	Ground
Pin 8	- $\overline{RAS}/\overline{OE}$ In	$\overline{RAS}$ Input from memory bus
Pin 9	- $\overline{CE}/\overline{CAS}$ Out	Chip enable or $\overline{CAS}$ to memory
Pin 10	- $\overline{CE}/\overline{CAS}$ In	Chip enable or $\overline{CAS}$ from memory bus
Pin 11	- CLK	Clock for serial port
Pin 12	- DQ	Data I/O for serial port
Pin 13	- $\overline{RST}$	Reset for serial port
Pin 14	- V_{CC}	+5 Volts

DESCRIPTION
The Phantom Interface is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a three wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. In this way, a sequence of software generated memory cycles encode commands and transfer data with low pin count. The serial port signaling is derived from the memory address bus

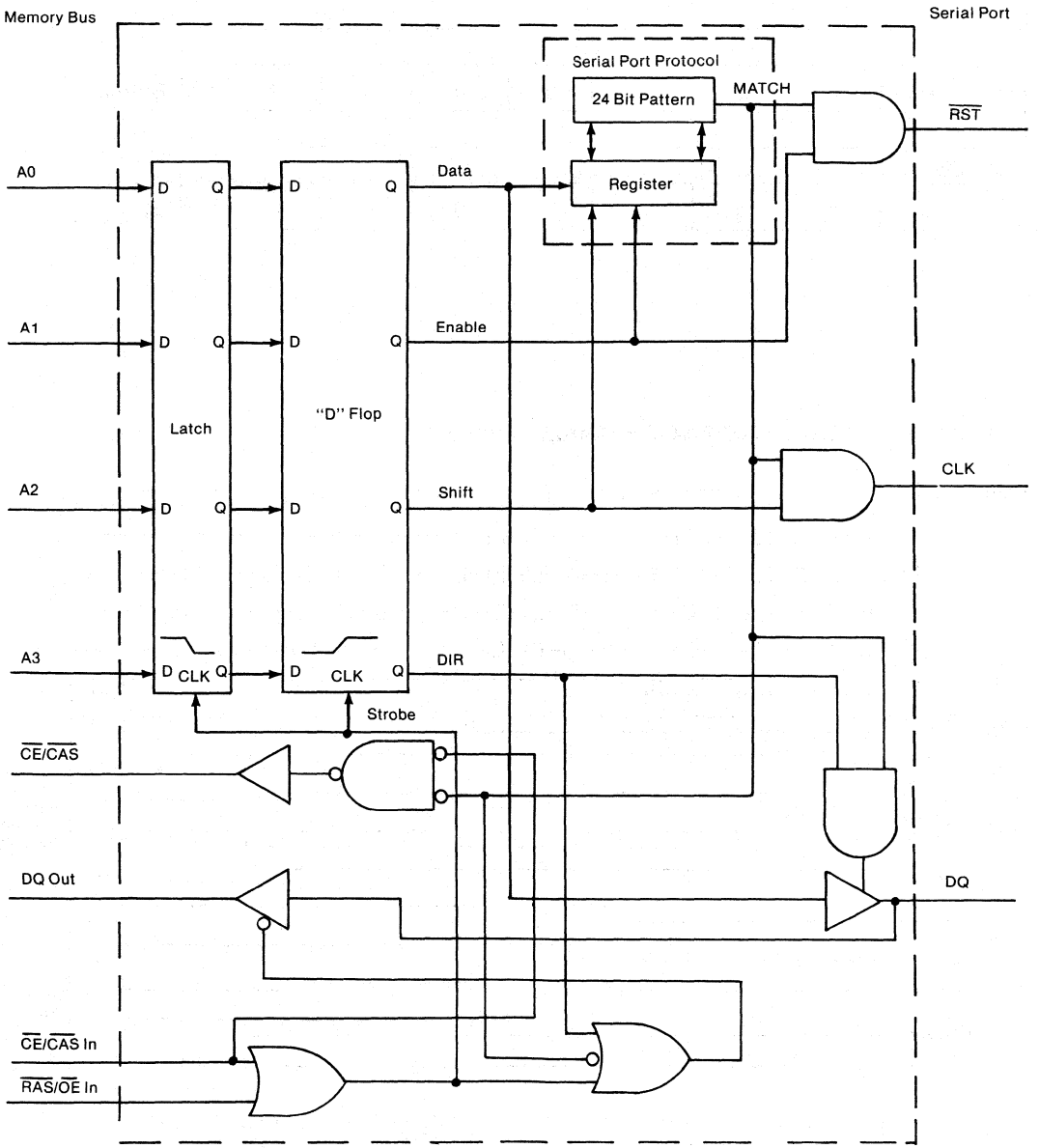
lines A0 through A3, the $\overline{CE}/\overline{CAS}$ signal and $\overline{RAS}/\overline{OE}$ signal, without affecting address space, thereby maintaining transparency to the memory bus. Communication is established under software control by an address pattern recognition sequence (serial port protocol) which disables a ByteWide or DRAM memory via $\overline{CE}/\overline{CAS}$ output. An additional address sequence is required to generate the three wire port signals: $\overline{RESET}$ ($\overline{RST}$), Data (DQ), and Clock (CLK). The add on serial port provides a minimum cost interface to the DS1201 Tag, the DS1204 Key, the DS1223 Configurator and the DS1290 Eliminator.

OPERATION

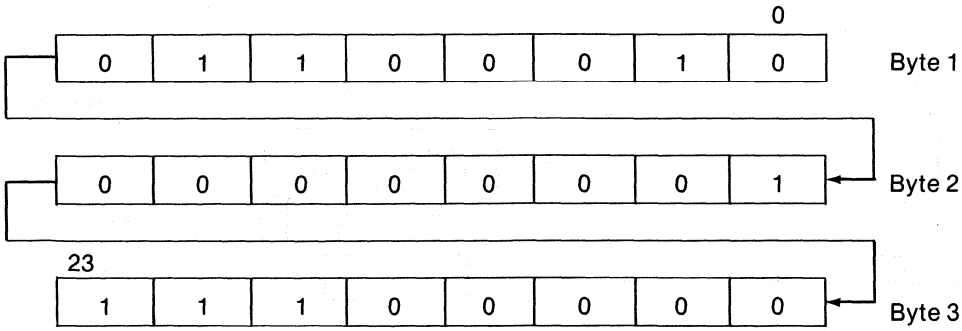
The main parts of the phantom serial interface are shown in the block diagram of Figure 1. Information presented on address inputs are latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}$ In and $\overline{RAS}/\overline{OE}$ In. When redirecting information from a DRAM memory bus, both $\overline{RAS}$ and $\overline{CAS}$ inputs are required and the column addresses are used for signaling. For a ByteWide memory bus, only a $\overline{CE}$ input is required and the $\overline{RAS}/\overline{OE}$ input can be tied low or connected to the memory $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2. A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24 bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Therefore, data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24 bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24 bit register for comparison to the 24 bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24 bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24 bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus. When $\overline{RST}$ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

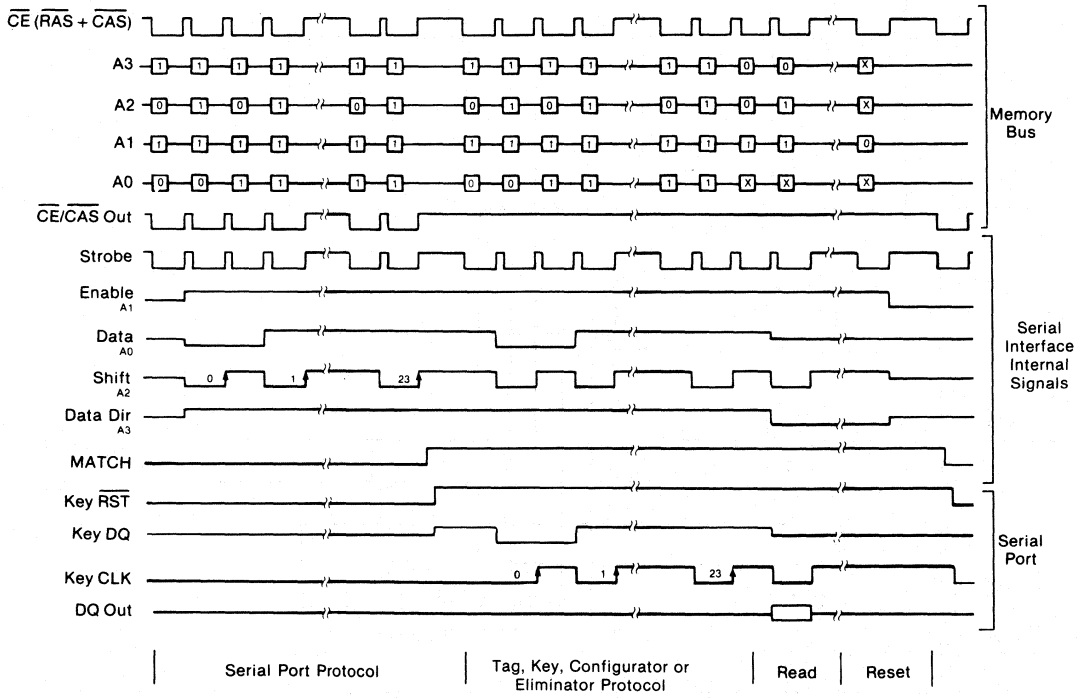
PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



PHANTOM SERIAL INTERFACE SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to +70°C
STORAGE TEMPERATURE	—	−40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	−0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1		1	A	
Output Leakage	I_{LO}			1	A	
Output Current @2.4V	I_{OH}	−1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

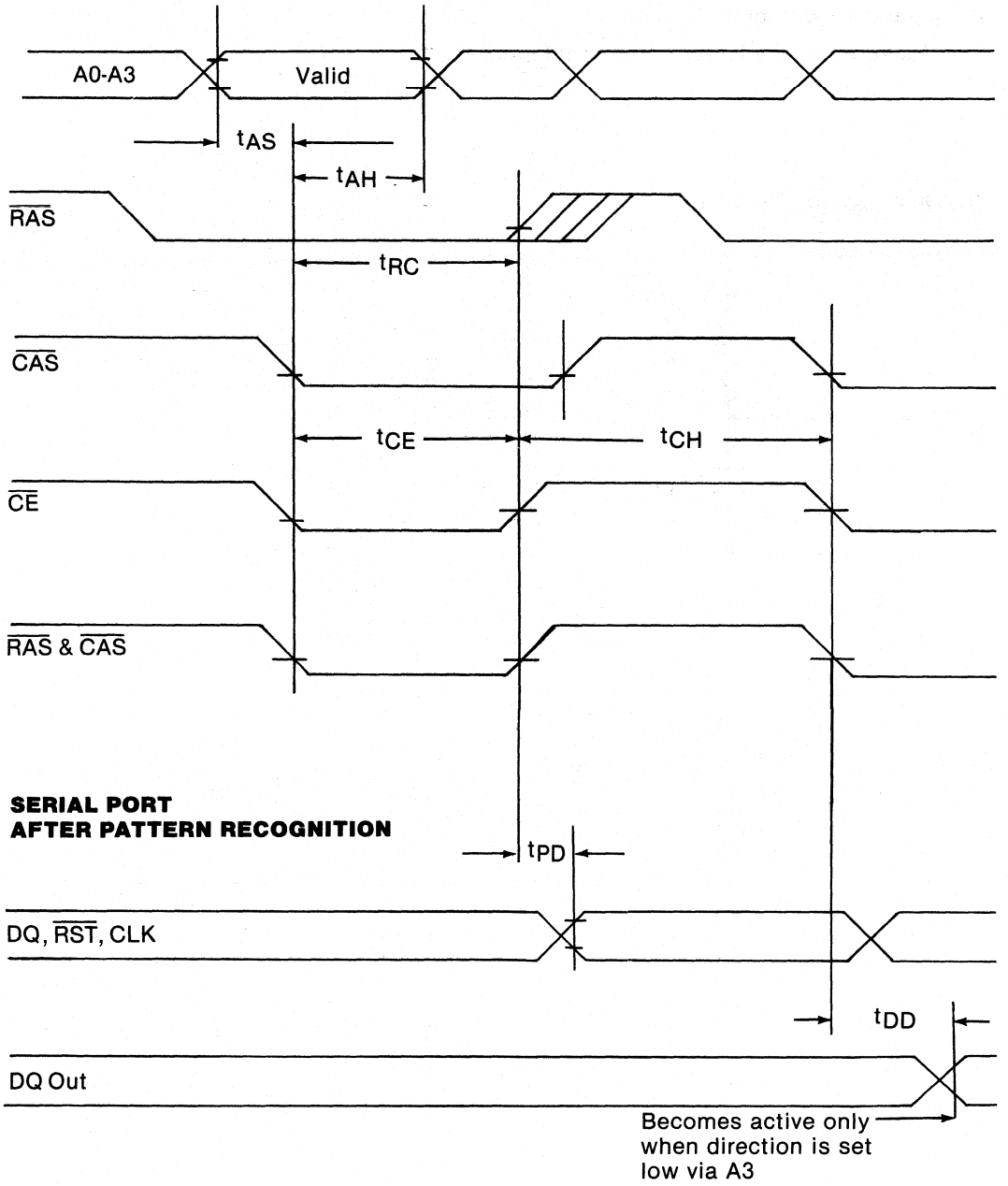
CAPACITANCE ($t_A = 25\,°C$)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Set Up	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{RAS}$ to $\overline{CAS}$ Overlap	t_{RC}	60			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	

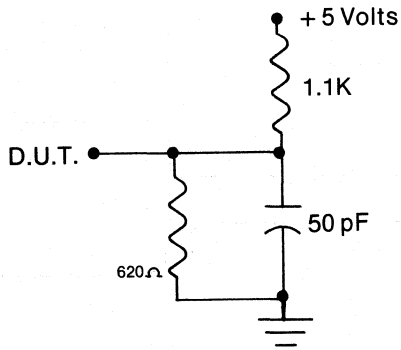
MEMORY BUS INPUTS



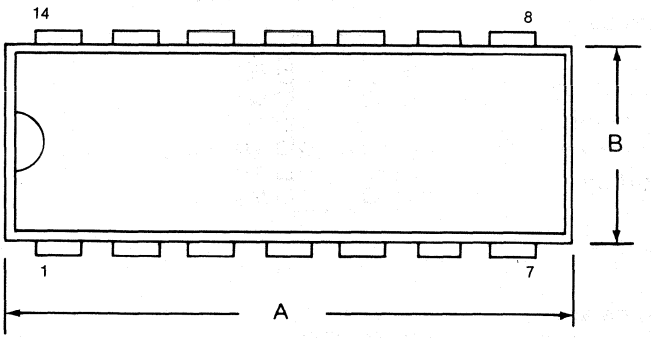
NOTES:

1. All voltages are referenced to ground
2. Measured with outputs open
3. Measured with a load as shown in Figure 4

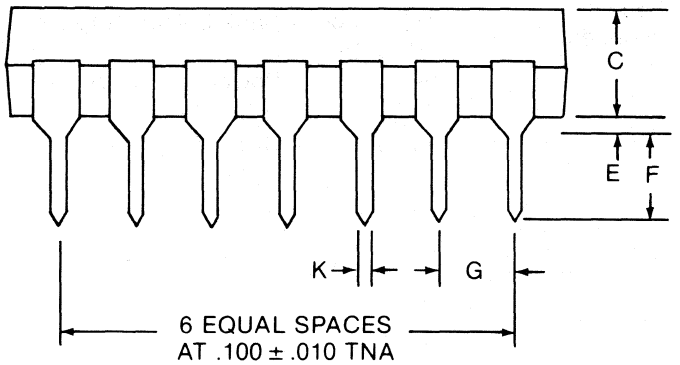
OUTPUT LOAD Figure 4

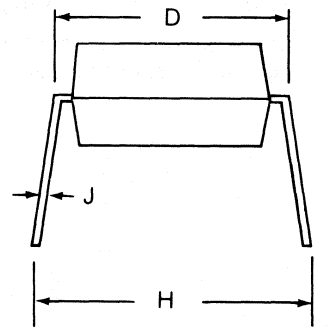


Phantom Serial Interface
DS1206



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021



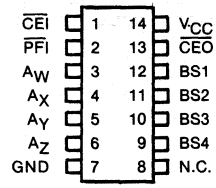


Dallas Semiconductor
BankSwitch

PRELIMINARY
DS1222

FEATURES
- Provides bank switching for 16 banks of memory
- Bank switching is software controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power up
- Bank switching logic allows only one bank on at a time
- Special custom recognition patterns are available which can prevent unauthorized access
- Full ±10% operating range
- Low power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders

PIN CONNECTIONS



PIN NAMES

A_W - A_Z	- Address Inputs
$\overline{CEI}$	- Chip Enable Input
$\overline{CEO}$	- Chip Enable Output
N.C.	- No Connection
BS1, BS2, BS3, BS4	- Bank Select Outputs
$\overline{PFI}$	- Power Fail Input
V_{CC}	- +5 Volts
GND	- Ground

DESCRIPTION

The DS1222 is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Special custom patterns are available from Dallas Semiconductor which can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212, up to 16 static RAMs can be selected in four different 32K-byte banks.

OPERATION—BANK SWITCHING

Initially, on power up all four bank select outputs are low and the chip enable output ($\overline{CEO}$) is held high. Note: the power fail input ($\overline{PFI}$) must be low prior to power-up to assure proper initialization. Bank siwtching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which will set the bank switch, a read cycle of 1111 on address inputs A_W through A_Z should be executed to guarantee that pattern entry starts with Bit 0. Each set of address inputs is clocked into the DS1222 when $\overline{CEI}$ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses A_X, A_Y, and A_Z. However, address line A_W defines the bank number to be enabled as per Table 2.

Switch to a selected bank of memory occurs on the rising edge of chip enable input when the last set of bits is input and a match has been established. After bank selection $\overline{CEO}$ always follows $\overline{CEI}$ with a maximum propagation delay of 15 ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

ADDRESS INPUT PATTERN Table 1

Address Inputs	Bit Sequence															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_W	1	0	1	0	0	0	1	1	0	1	0	×	×	×	×	×
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

× See Table 2

BANK SELECT CONTROL Table 2

Bank Selected	A_W Bit Sequence					Outputs			
	11	12	13	14	15	BS1	BS2	BS3	BS4
*Banks Off	0	×	×	×	×	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*$\overline{CEO} = V_{IH}$ independent of $\overline{CEI}$

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	−0.3V to +7.0V
OPERATING TEMPERATURE	0°C to 70°C
STORAGE TEMPERATURE	−40°C to +85°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Input Low Voltage	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	*u*A	
I/O Leakage Current	I_{LO}	−1.0		+1.0	*u*A	
Output Current @2.4V	I_{OH}	−1.0			mA	
Output Current @0.4V	I_{OL}			+4.0	mA	
Operating Current	I_{CC}			15	mA	

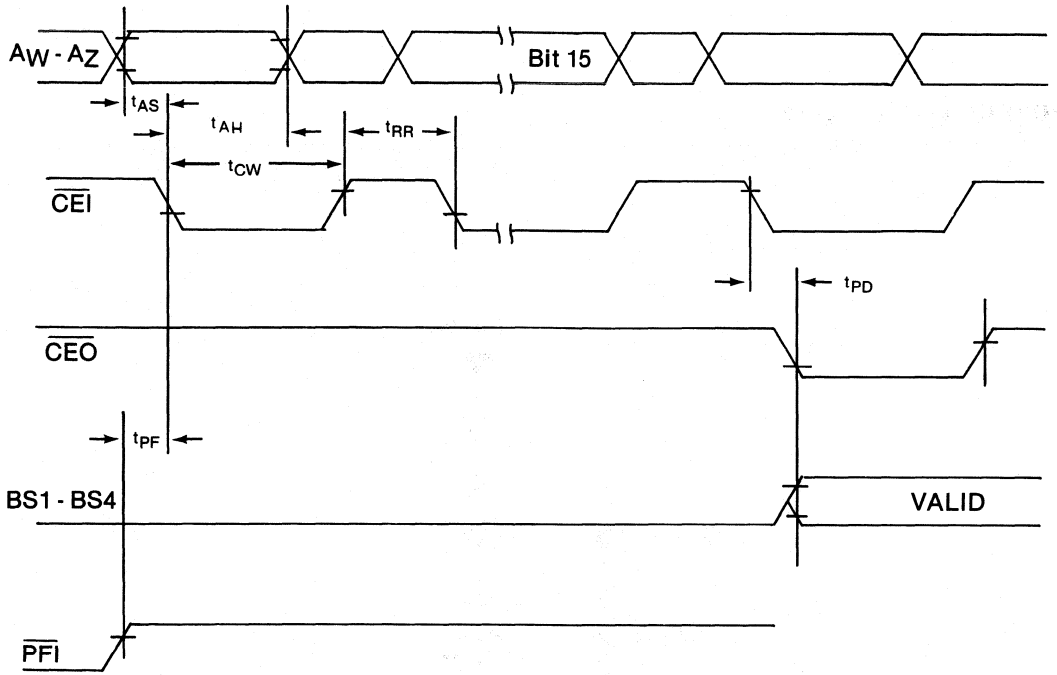
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	TYP.	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Address Set-Up	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	
Power Fail Input to First CEI	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

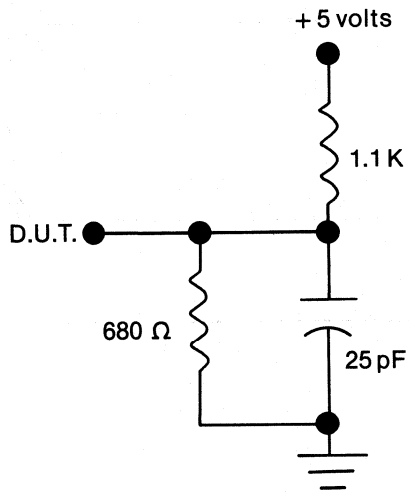
TIMING DIAGRAM—ACCESS TO BANK SWITCH



NOTES: 1. All voltages are referenced to ground.

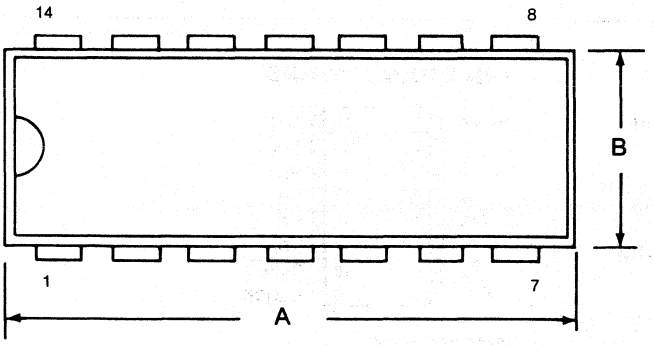
2. Measured with a load as shown in Figure 1.

OUTPUT LOAD Figure 1

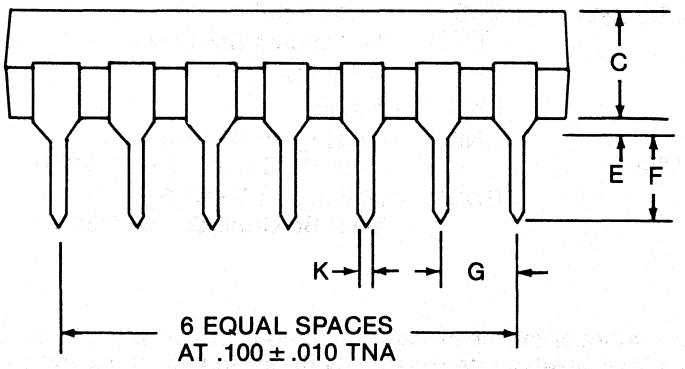


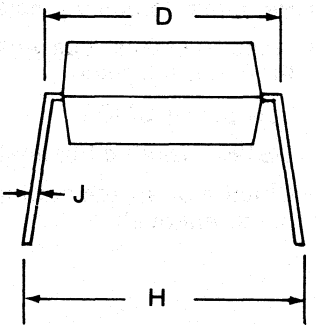
Output Load

Bank Select Controller
DS1222



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021





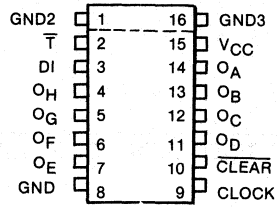
Dallas Semiconductor
Eliminator

DS1290
DS1291

FEATURES

- Replaces 8 hard-to-get-at manual switches
- Option printed circuit board via software
- DS1290 remembers settings in the absence of power
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Interface
- Low power CMOS
- DS1291 Volatile Eliminator
- Change of switch settings occur simultaneously

PIN CONNECTIONS



PIN NAMES

$\overline{T}$	- Transfer
DI	- Data Input
O_AO_H	- Switch Outputs
CLOCK	- Clock Input
$\overline{CLEAR}$	- All Outputs Set Low
V_{CC}	- +5 Volts
GND	Ground
GND2	- Missing on DS1290 Must Be Grounded on DS1291
GND3	- Missing on DS1290 Must Be Grounded on DS1291

DESCRIPTION

The DS1290 Eliminator replaces manual switches used to option printed circuit boards. Eight output pins can be set to a logic level or interrogated by three signals, clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 will maintain high or low level output duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

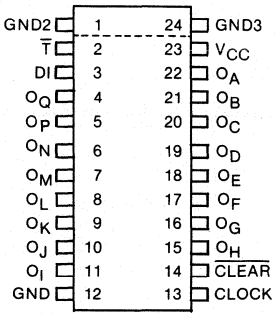
Dallas Semiconductor
Eliminator

DS1292
DS1293

FEATURES

- Replaces 16 hard-to-get-at manual switches
- Option printed circuit board via software
- DS1292 remembers settings in the absence of power
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Interface
- Low power CMOS
- DS1293 Volatile Eliminator
- Change of switch settings occur simultaneously

PIN CONNECTIONS



PIN NAMES

$\overline{T}$	- Transfer
DI	- Data Input
O_AO_Q	- Switch Outputs
CLOCK	- Clock Input
$\overline{CLEAR}$	- All Outputs Set Low
V_{CC}	- +5 Volts
GND	- Ground
GND2	- Missing on DS1292 Must Be Grounded on DS1293
GND3	- Missing on DS1292 Must Be Grounded on DS1293

DESCRIPTION

The DS1292 Eliminator replaces manual switches used to option printed circuit boards. Sixteen output pins can be set to a logic level or interrogated by three signals, clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1292 will maintain high or low level output duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

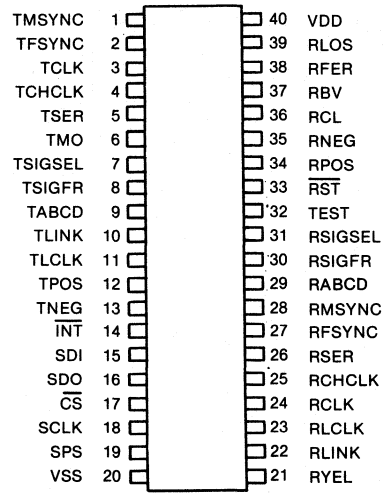
Dallas Semiconductor
Serial T1 Transceiver

PRELIMINARY
DS2180

FEATURES

- Single chip DS1 rate transceiver
- Supports common framing standards
  - -12 frames/superframe "193S"
  - -24 frames/superframe "193E"
- Three zero suppression modes
  - -B7 stuffing
  - -B8ZS
  - -Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology

PIN CONNECTIONS



DESCRIPTION

The DS2180 is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

Several functional blocks exist in the transceiver. The transmit framer/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

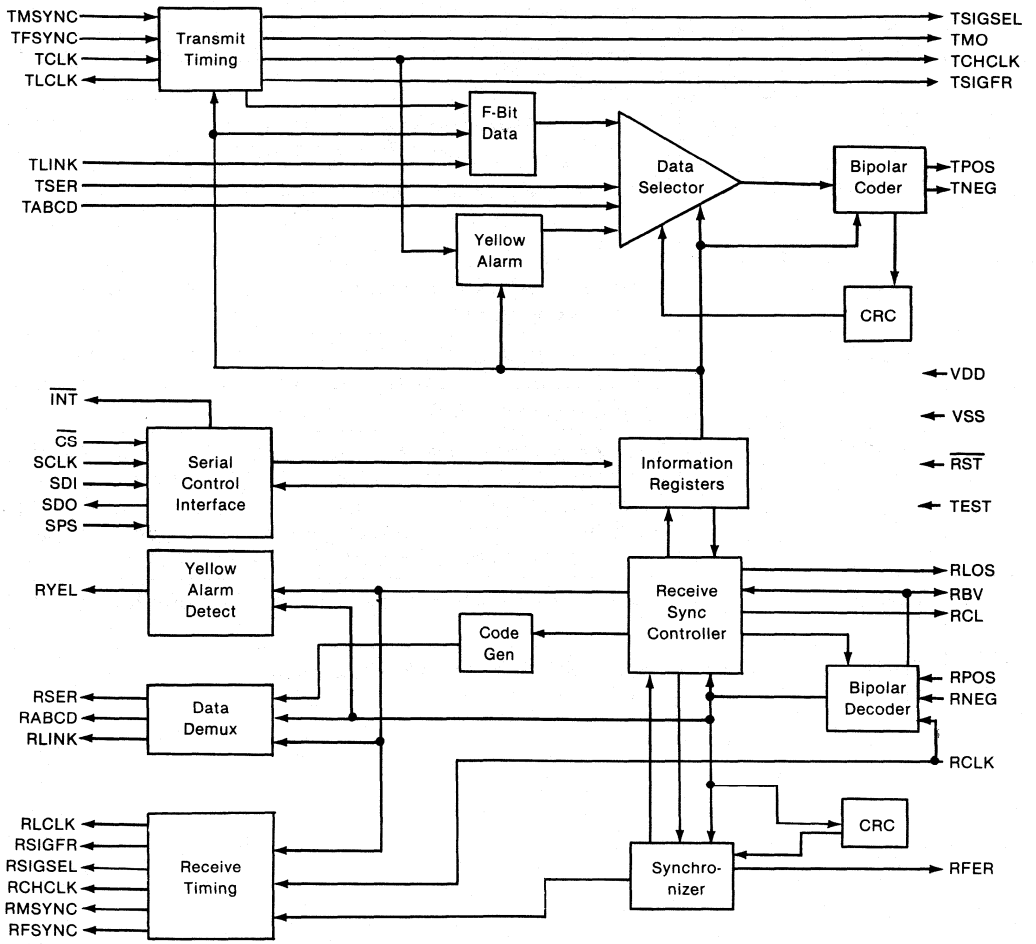
The receive synchronizer establishes frame and multiframe boundaries by identifying frame signaling bits, extracts signaling data, reports alarms and transmission errors, and provides output clocks useful for data conditioning and decoding.

The control block is shared between transmit and receive sides. This block determines the frame, zero suppression, alarm and signaling formats. User access to the control block is by one of two modes.

In the processor mode pins 14 through 18 are a microprocessor/microcontroller compatible serial port which can be used for device configuration, control and status monitoring.

In the hardware mode no offboard processor is required. Pins 14 through 18 are reconfigured into "hardwired" select pins. Features such as selective "clear" DS0 channels, insertion of idle code and alteration of sync algorithm are unavailable in the hardware mode.

DS2180 BLOCK DIAGRAM Figure 1



TRANSMIT PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**TMSYNC**	I	**Transmit Multiframe Sync.** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	**TFSYNC**	I	**Transmit Frame Sync.** Rising edge identifies frame boundary; may be pulsed every frame to reinforce internal frame counter, or tied low (allowing TMSYNC to establish frame and multiframe alignment).
3	**TCLK**	I	**Transmit Clock.** 1.544 MHz primary clock.
4	**TCHCLK**	O	**Transmit Channel Clock.** 192 KHz clock which identifies time slot (channel) boundaries. Useful for parallel to serial conversion of channel data.
5	**TSER**	I	**Transmit Serial Data.** NRZ data input, sampled on falling edge of TCLK.
6	**TMO**	O	**Transmit Multiframe Out.** Output of internal multiframe counter, indicates multiframe boundaries. 50% duty cycle.
7	**TSIGSEL**	O	**Transmit Signaling Select.** .667 KHz clock which identifies signaling frames A and C in 193E framing. 1.33 KHz clock in 193S.
8	**TSIGFR**	O	**Transmit Signaling Frame.** High during signaling frames, low otherwise.
9	**TABCD**	I	**Transmit ABCD Signaling.** When enabled via TCR.4, sampled during channel LSB time in signaling frames on falling edge of TCLK.
10	**TLINK**	I	**Transmit Link Data.** Sampled during the F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-Bit insertion).
11	**TLCLK**	O	**Transmit Link Clock.** 4 KHz demand clock for TLINK input.
12 13	**TPOS** **TNEG**	O	**Transmit Bipolar Data Outputs.** Updated on rising edge of TCLK.

PORT PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
14	$\overline{\text{INT}}$[1]	O	**Receive Alarm Interrupt.** Flags host controller during alarm conditions. Active low, open drain output.
15	SDI[1]	I	**Serial Data In.** Data for on-board registers. Sampled on rising edge of SCLK.
16	SDO[1]	O	**Serial Data Out.** Control and status information from on-board registers. Updated on falling edge of SCLK, tri-stated during serial port write or when $\overline{\text{CS}}$ is high.
17	$\overline{\text{CS}}$[1]	I	**Chip Select.** Must be low to write or read the serial port.
18	SCLK[1]	I	**Serial Data Clock.** Used to write or read the serial port registers.
19	SPS	I	**Serial Port Select.** Tie to VDD to select serial port. Tie to VSS to select hardware mode.
NOTES: 1. Multifunction pins, see hardware mode description.			

POWER AND TEST PIN DESCRIPTION Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
20	VSS	-	**Signal Ground.** 0.0 volts.
32	TEST	I	**Test Mode.** Tie to VSS for normal operation.
40	VDD	-	**Positive Supply.** 5.0 volts.

RECEIVE PIN DESCRIPTION Table 4

PIN	SYMBOL	TYPE	DESCRIPTION
21	**RYEL**	O	**Receive Yellow Alarm.** Transitions high when yellow alarm detected, goes low when alarm clears.
22	**RLINK**	O	**Receive Link Data.** Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	**RLCLK**	O	**Receive Link Clock.** 4 KHz demand clock for RLINK.
24	**RCLK**	I	**Receive Clock.** 1.544 MHz primary clock.
25	**RCHCLK**	O	**Receive Channel Clock.** 192 KHz clock, identifies time slot (channel) boundaries.
26	**RSER**	O	**Receive Serial Data.** Received NRZ serial data, updated on rising edges of RCLK.
27	**RFSYNC**	O	**Receive Frame Sync.** Extracted 8 KHz clock, one RCLK wide, indicates F-Bit position in each frame.
28	**RMSYNC**	O	**Receive Multiframe Sync.** Extracted multiframe sync; edge indicates start of multiframe, 50% duty cycle.
29	**RABCD**	O	**Receive ABCD Signaling.** Extracted signaling data output, valid for each channel time in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
30	**RSIGFR**	O	**Receive Signaling Frame.** High during signaling frames, low during resync and non-signaling frames.
31	**RSIGSEL**	O	**Receive Signaling Select.** In 193E framing a .667 KHz clock which identifies signaling frames A and C. A 1.33 KHz clock in 193S.
33	**$\overline{\text{RST}}$**	I	**Reset.** A high-low transition clears all internal registers and resets receive side counters. A high-low-high transition will initiate a receive resync.
34 35	**RPOS** **RNEG**	I	**Receive Bipolar Data Inputs.** Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
36	**RCL**	O	**Receive Carrier Loss.** High if 32 consecutive "0's" appear at RPOS and RNEG, goes low after next "1."
37	**RBV**	O	**Receive Bipolar Violation.** High during accused bit time at RSER if bipolar violation detected, low otherwise.

38	**RFER**	O	**Receive Frame Error.** High during F-Bit time when F_T or F_S errors occur (193S), or when FPS or CRC errors occur (193E). Low during resync.
39	**RLOS**	O	**Receive Loss of Sync.** Indicates sync status; high when internal resync is in progress, low otherwise.

REGISTER SUMMARY Table 5

REGISTER	ADDRESS	T/R[1]	DESCRIPTION/FUNCTION
RSR	0000	R[2]	**Receive Status Register.** Reports all receive alarm conditions.
RIMR	0001	R	**Receive Interrupt Mask Register.** Allows masking of individual alarm generated interrupts.
BVCR	0010	R	**Bipolar Violation Count Register.** 8 bit presettable counter which records individual bipolar violations.
ECR	0011	R	**Error Count Register.** 2 independent 4-bit counters which record OOF occurrences, and individual frame bit or CRC errors.
CCR[3]	0100	T/R	**Common Control Register.** Selects device operating characteristics common to receive and transmit sides.
RCR[3]	0101	R	**Receive Control Register.** Programs device operating characteristics unique to the receive side.
TCR[3]	0110	T	**Transmit Control Register.** Selects additional transmit side modes.
TIR1 **TIR2** **TIR3**	0111 1000 1001	T T T	**Transmit Idle Registers.** Designate which outgoing channels are to be substituted with idle code.
TTR1 **TTR2** **TTR3**	1010 1011 1100	T T T	**Transmit Transparent Registers.** Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
RMR1 **RMR2** **RMR3**	1101 1110 1111	R R R	**Receive Mark Registers.** Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control of RCR).

NOTES: 1. Transmit or receive side register.
2. RSR is a read only register, all other registers are read/write.
3. Reserved bit locations in the control registers should be programmed to 0, to maintain compatibility with future transceiver products.

SERIAL PORT INTERFACE
Pins 14 through 18 of the DS2180 serve as a microprocessor/microcontroller compatible serial port. Sixteen on-board registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads and/or writes by the host.

ADDRESS/COMMAND
Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. The following 4 bit nibble identifies register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. *Data is written to and read from the transceiver LSB first.*

CHIP SELECT AND CLOCK CONTROL
All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the rising edge of SCLK and *must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes.* Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is tristated when $\overline{CS}$ is high.

DATA I/O
Following the 8 SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edges of the next 8 SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next 8 SCLK cycles. The SDO pin is tristated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE
The burst mode allows all on-board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power-up or system reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. Burst is terminated by low-high transition on $\overline{CS}$.

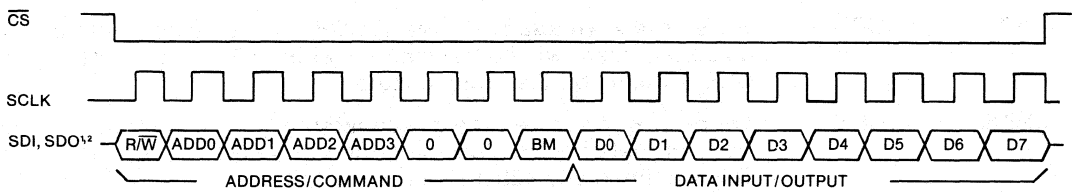
ACB: ADDRESS COMMAND BYTE Figure 2

(MSB) (LSB)

BM	—	—	ADD3	ADD2	ADD1	ADD0	R/$\overline{W}$

SYMBOL	POSITION	NAME AND DESCRIPTION
BM	ACB.7	**Burst Mode.** If set (and ACB.1 through ACB.4 = 0) burst read or write is enabled
—	ACB.6	Reserved, must be 0 for proper operation
—	ACB.5	Reserved, must be 0 for proper operation
ADD3	ACB.4	MSB of register address
ADD0	ACB.1	LSB of Register address
R/$\overline{W}$	ACB.0	**Read/Write Select.** 0 = write addressed register 1 = read addressed register

SERIAL PORT READ/WRITE Figure 3



NOTES: 1. SDI sampled on rising edge of SCLK
2. SDO updated on falling edge of SCLK

COMMON CONTROL REGISTER Figure 4

(MSB) (LSB)

—	—	—	FM	YELMD	B8ZS	B7	LPBK

SYMBOL	POSITION	NAME AND DESCRIPTION
—	CCR.7	Reserved, must be 0 for proper operation
—	CCR.6	Reserved, must be 0 for proper operation
—	CCR.5	Reserved, must be 0 for proper operation
FM	CCR.4	**Frame Mode Select.** 0 = D4 (193S, 12 frames/superframe) 1 = Extended (193E, 24 frames/superframe)
YELMD	CCR.3	**193S Yellow Mode Select.** Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12; if cleared, yellow alarm is a "0" in bit 2 of all channels. Does not affect 193E yellow alarm operation.
B8ZS	CCR.2	**Bipolar eight zero substitution.** 0 = No B8ZS 1 = B8ZS Enabled
B7	CCR.1	**Bit seven zero suppression.** If CCR.1 = 1, channels with an all zero content will be transmitted with bit 7 forced to "1." If CCR.1 = 0, no bit 7 stuffing occurs.
LPBK	CCR.0	**Loopback.** When set, the device internally loops output transmit data into the incoming receive data buffers and TCLK is internally substituted for RCLK.

LOOPBACK

Enabling loopback will typically induce an out-of-frame "OOF" condition. If appropriate bits are set in the receive control register, the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit unframed all "1's." All operating modes (B8ZS, alarm, signaling, etc.) except for blue alarm transmission are available in loopback.

BIT SEVEN STUFFING

Existing systems meet one's density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is "globally" enabled by asserting bit CCR.1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1-TTR3.

B8ZS

The DS2180 supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system one's density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces 8 consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

TCR: TRANSMIT CONTROL REGISTER Figure 5

(MSB) (LSB)

—	—	TCP	RBSE	TIS	193SI	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION
—	TCR.7	Reserved, must be 0 for proper operation.
—	TCR.6	Reserved, must be 0 for proper operation
TCP	TCR.5	**Transmit CRC Pass-through.** 0 = Transmit CRC code internally generated. 1 = TSER sampled at CRC F-bit time for external CRC insertion.
RBSE	TCR.4	**Robbed Bit Signaling Enable.** 1 = signaling inserted in all channels during signaling frames. 0 = no signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DS0 channels.)
TIS	TCR.3	**Transmit Idle Code Select.** Determines idle code format to be inserted into channels marked by the TIR registers. 0 = insert 7F (Hex) into marked channels. 1 = insert FF (Hex) into marked channels.
193SI	TCR.2	**193S S-bit Insertion.** Determines source of transmitted S-bit. 0 = internal S-bit generator 1 = external (sampled at TLINK input)
TBL	TCR.1	**Transmit Blue Alarm.** 0 = disabled 1 = enabled
TYEL	TCR.0	**Transmit Yellow Alarm.** 0 = disabled 1 = enabled

TRANSMIT BLUE ALARM

The blue alarm (also known as the AIS, Alarm Indication Signal) is an unframed, all 1's sequence enabled by asserting TCR.1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR.1. Use of the TIR registers allows a framed, all 1's alarm transmission if required by the network.

TRANSMIT YELLOW ALARM

In 193E framing a yellow alarm is a repeating pattern set of FF (Hex) and 00 (Hex) on the 4 KHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of bit CCR.3. In all modes, yellow alarm is enabled by asserting TCR.0 and disabled by clearing TCR.0.

TRANSMIT SIGNALING

When enabled (via TCR.4) channel signaling is inserted in frames 6 and 12, (193S) or 6, 12 and 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate serial links for A, B or A, B, C, D signaling sources.

TTR1-TTR3: TRANSMIT TRANSPARENCY REGISTERS Figure 6

(MSB) (LSB)

CH8	**CH7**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**	TTR1
CH16	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH9**	TTR2
CH24	**CH23**	**CH22**	**CH21**	**CH20**	**CH19**	**CH18**	**CH17**	TTR3

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	**Transmit Transparent Registers.** Each of these bit positions represents a DS0 channel in the outgoing frame. When set the corresponding channel is transparent.
CH1	TTR1.0	

TIR1-TIR3: TRANSMIT IDLE REGISTERS Figure 7

(MSB) (LSB)

CH8	**CH7**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**	TIR1
CH16	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH9**	TIR2
CH24	**CH23**	**CH22**	**CH21**	**CH20**	**CH19**	**CH18**	**CH17**	TIR3

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	**Transmit Idle Registers.** Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR.3.
CH1	TIR1.0	

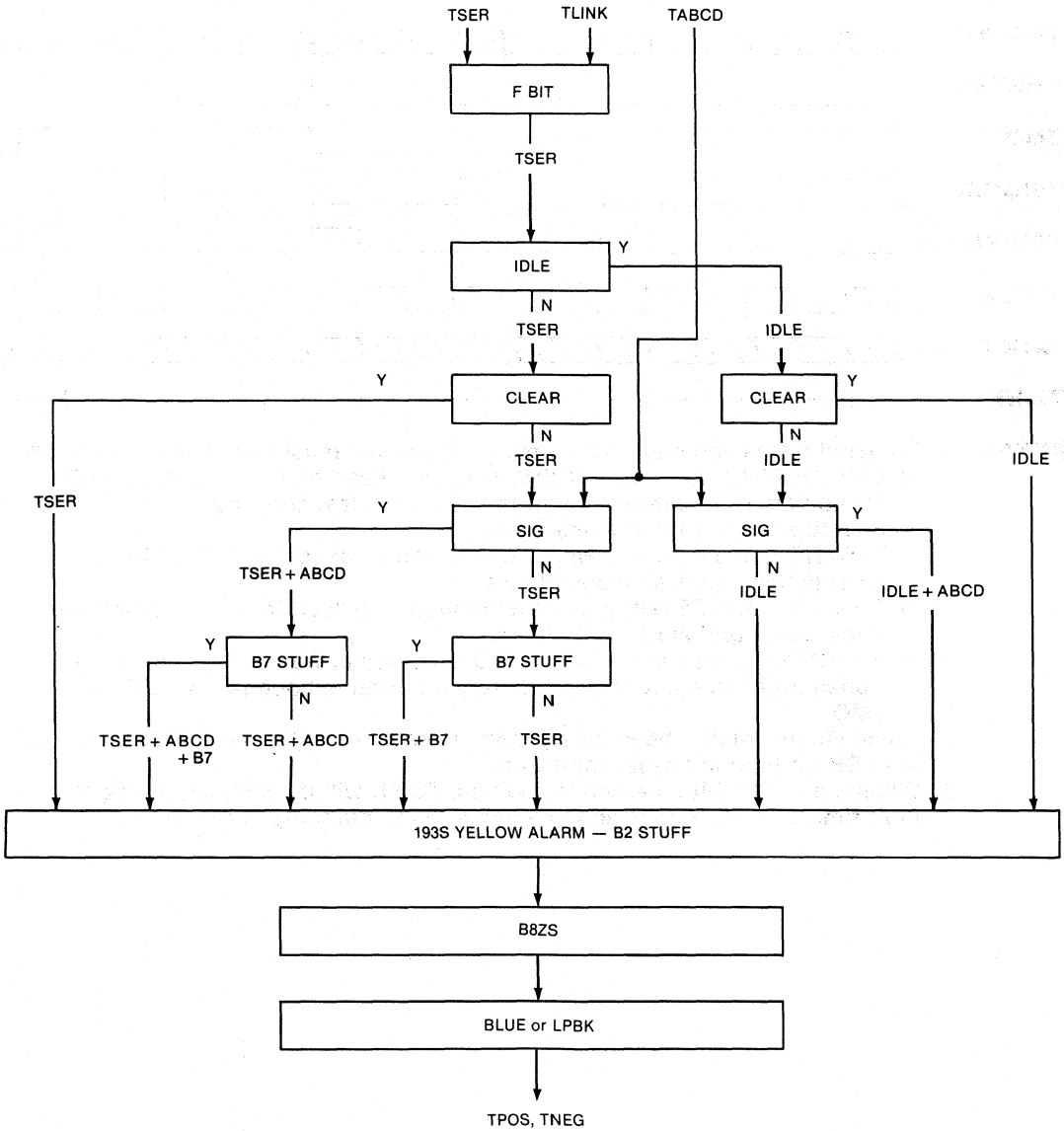
TRANSMIT CHANNEL TRANSPARENCY

Individual DS0 channels in the T1 frame may be programmed clear (no inserted robbed bit signaling and no bit 7 zero suppression) by setting the appropriate bits in the transmit transparency registers. Channel transparency is required in mixed voice/data or data-only environments such as ISDN, where data integrity must be maintained.

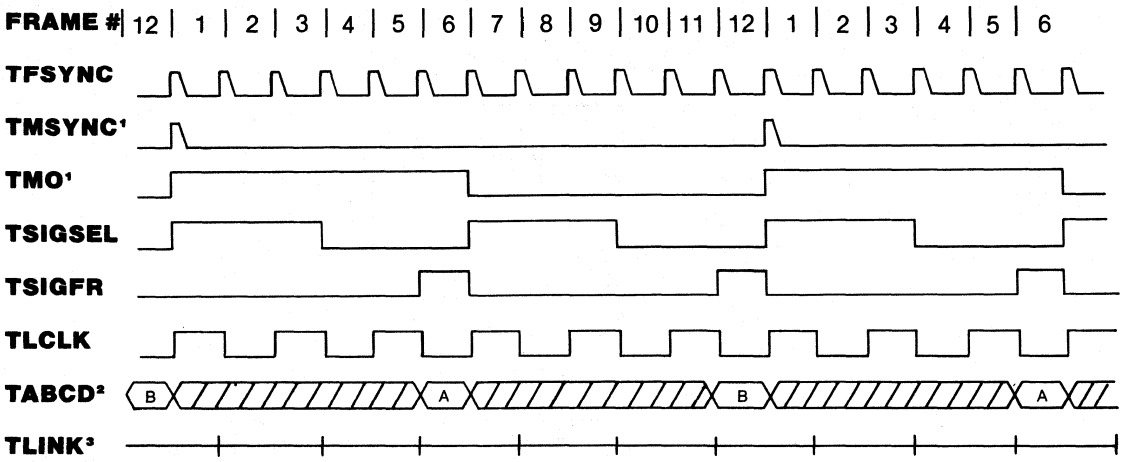
TRANSMIT IDLE CODE INSERTION

Individual outgoing channels in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR.3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates external hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream.

TRANSMIT INSERTION HIERARCHY Figure 8



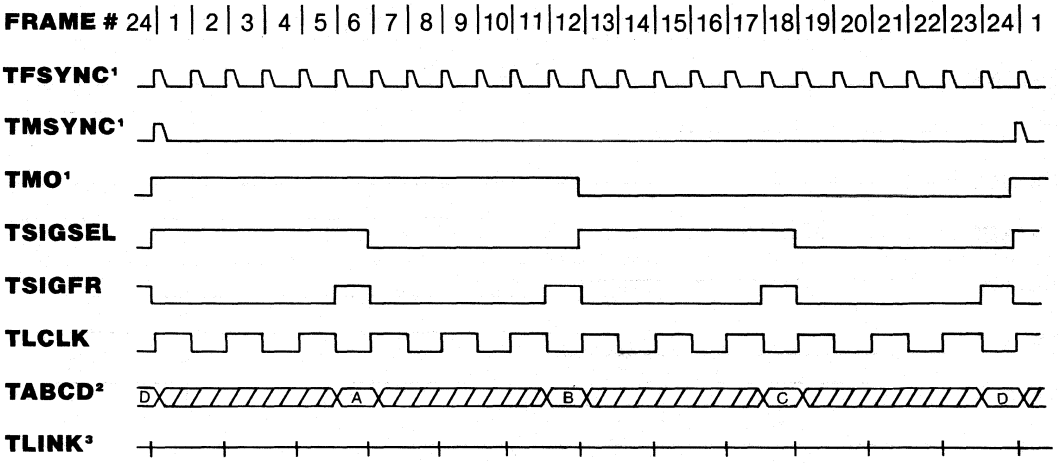
193S TRANSMIT MULTIFRAME TIMING Figure 9



NOTES:

1. Transmit frame and multiframe timing may be established in one of four ways:
   a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c) TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
   d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. When external S-bit insertion is enabled, TLINK will be sampled during the F-bit time of even frames and inserted into the outgoing data stream.

193E TRANSMIT MULTIFRAME TIMING Figure 10



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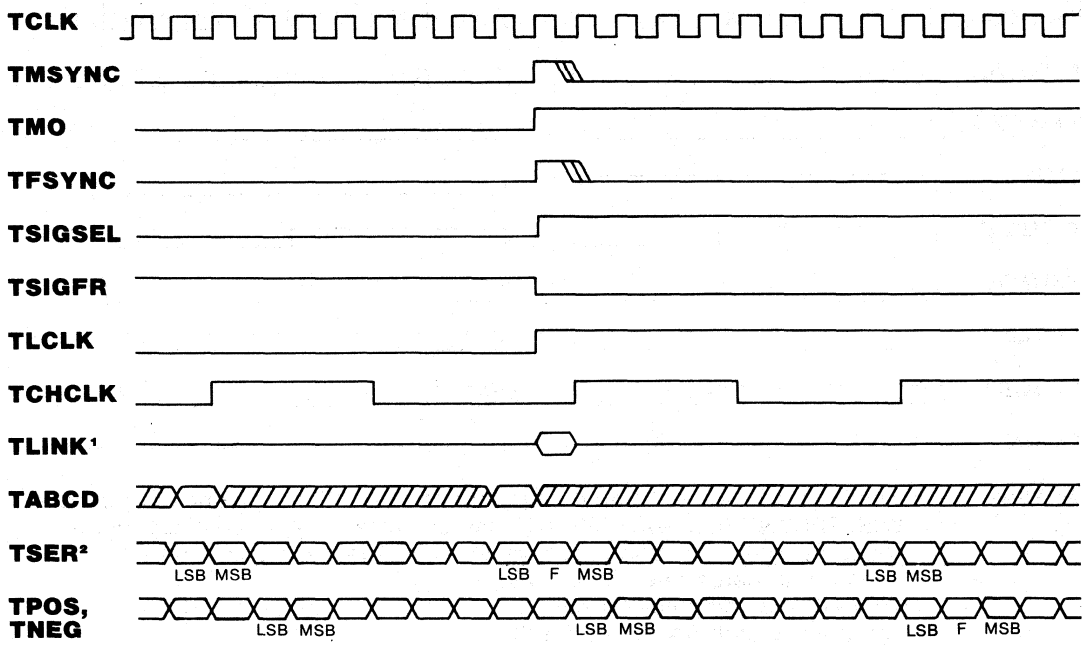
   d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. TLINK is sampled during the F-bit time of odd frames and inserted into the outgoing data stream (FDL data).

TRANSMIT MULTIFRAME BOUNDARY TIMING Figure 11



NOTES: 1. TLINK timing shown is for 193E framing; in 193E framing, TLINK is sampled as indicated for insertion into F-bit position of odd frames. When S-bit insertion is enabled in 193S, TLINK is sampled during even frames.

2. If TCR.5 = 1; TSER is sampled during the F-bit time of CRC frames for insertion into the outgoing data stream (193E Framing only).

RECEIVE CONTROL REGISTER Figure 12

(MSB) (LSB)

—	—	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
—	RCR.7	Reserved, must be 0 for proper operation
—	RCR.6	Reserved, must be 0 for proper operation
RCI	RCR.5	**Receive Code Insert.** When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.
RCS	RCR.4	**Receive Code Select.** 0 = idle code (7F Hex) 1 = digital milliwatt
SYNCC	RCR.3	**Sync Criteria.** Determines the type of algorithm utilized by the receive synchronizer and differs for each frame mode. **193S Framing (CCR.4 = 0).** 0 = synchronize to frame boundaries using F_T pattern, then search for multiframe by using F_S. 1 = cross couple F_T and F_S patterns in sync algorithm. **193E Framing (CCR.4 = 1).** 0 = normal sync (utilizes FPS only) 1 = validate new alignment with CRC before declaring sync.
SYNCT	RCR.2	**Sync Time.** If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.
SYNCE	RCR.1	**Sync Enable.** If clear, the transceiver will automatically begin a resync if 2 of the previous 4 framing bits were in error, or if carrier loss is detected. If set, no auto resync occurs.
RESYNC	RCR.0	**Resync.** When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

RECEIVE CODE INSERTION

Incoming receive channels can be replaced with idle (7F Hex) or digital milliwatt (u-LAW format) codes. The receive mark registers indicate which channels are inserted. When set, bit RCR.5 serves as a "global" enable for marked channels, and bit RCR.4 selects inserted code format: 0 = idle code, 1 = digital milliwatt.

RECEIVE SYNCHRONIZER

Bits RCR.0 through RCR.3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate qualify testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

RECEIVE SIGNALING

Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

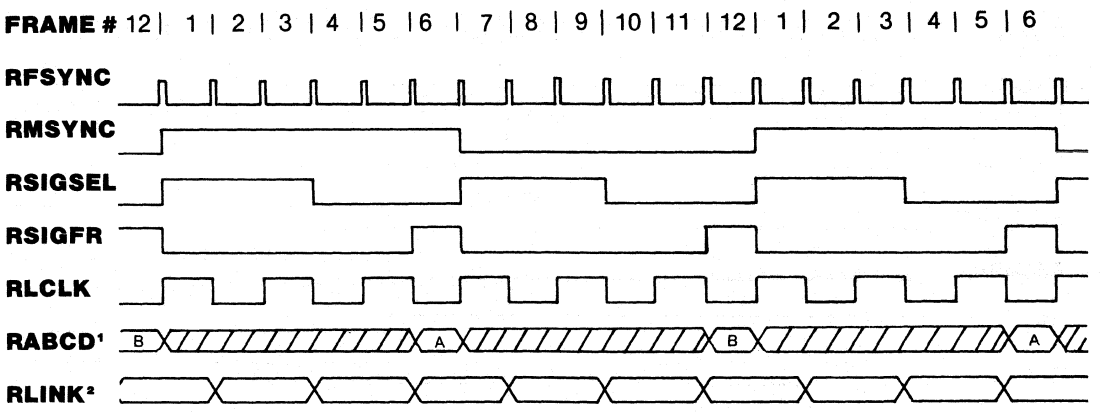
RMR1-RMR3: RECEIVE MARK REGISTERS Figure 13

(MSB) (LSB)

CH8	**CH7**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**	RMR1
CH16	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH9**	RMR2
CH24	**CH23**	**CH22**	**CH21**	**CH20**	**CH19**	**CH18**	**CH17**	RMR3

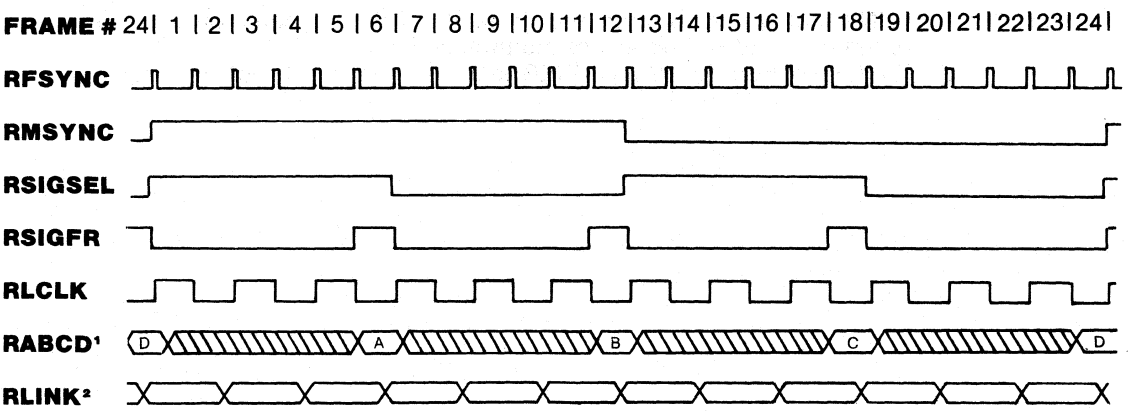
SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RMR3.7	**Receive Mark Registers.** Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set the corresponding channel will output codes determined by RCR.4 and RCR.5.
CH1	RMR1.0	

193S RECEIVE MULTIFRAME TIMING Figure 14



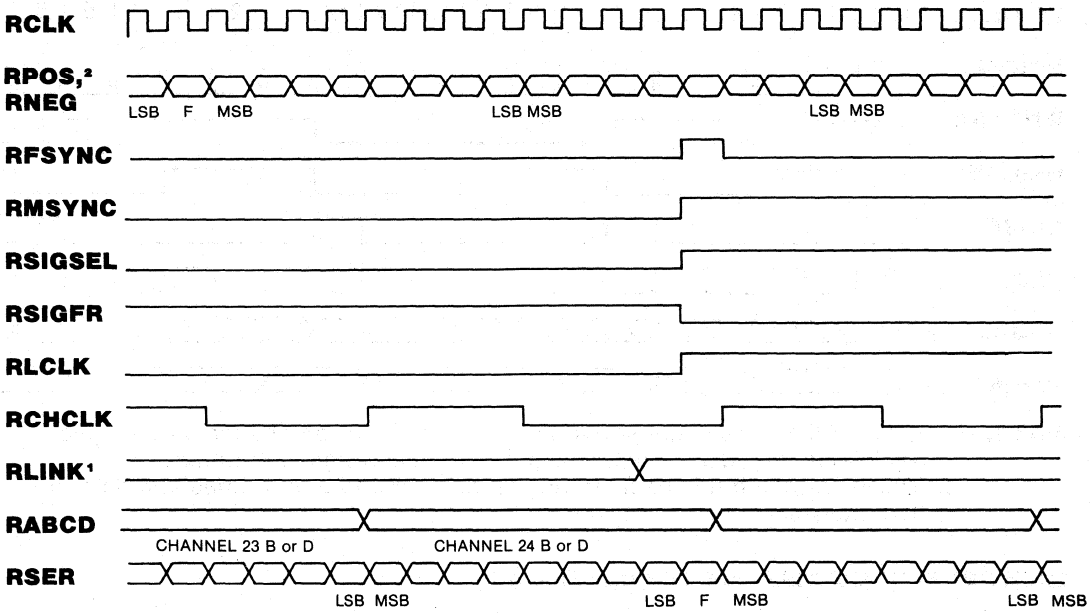
NOTES: 1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

193E RECEIVE MULTIFRAME TIMING Figure 15



NOTES: 1. Signaling data is updated during signaling frames on channel boundaries. RABCD outputs the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit time prior to odd frames and held for two frames.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 16



NOTES: 1. RLINK timing is shown for 193E; in 193S RLINK is updated on even frame boundaries and is held across multiframe edges.
2. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.

RSR: RECEIVE STATUS REGISTER Figure 17

(MSB) (LSB)

BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
BVCS	RSR.7	**Bipolar Violation Count Saturation.** Set when the 8-bit counter at BVCR saturates.
ECS	RSR.6	**Error Count Saturation.** Set when either of the 4-bit counters at ECR saturates.
RYEL	RSR.5	**Receive Yellow Alarm.** Set when yellow alarm detected. (Detected yellow alarm format determined by CCR.4 and CCR.3.)
RCL	RSR.4	**Receive Carrier Loss.** Set when 32 consecutive "0's" appear at RPOS and RNEG.
FERR	RSR.3	**Frame Bit Error.** Set when F_T (193S) or FPS (193E) bit error occurs.
B8ZSD	RSR.2	**Bipolar Eight Zero Substitution Detect.** Set when B8ZS code word detected.
RBL	RSR.1	**Receive Blue Alarm.** Set when 2 consecutive frames have less than 3 zeros (total) in the data stream (F-bit positions not tested).
RLOS	RSR.0	**Receive Loss of Sync.** Set when resync is in process; if RCR.1 = 0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

RECEIVE ALARM REPORTING

Incoming serial data is monitored by the transceiver for alarm occurrences. Alarm conditions are reported in two ways: via transitions on the alarm output pins and registered interrupt, in which the host controller reads the RSR in response to an alarm driven interrupt. Interrupts may be direct, in which the transceiver demands service for a real time alarm, or count-overflow triggered, in which an on-board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register (RIMR).

ALARM SERVICING

The host controller must service the transceiver in order to clear an interrupt condition. Clearing appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupts (those driven from real-time alarms) will be cleared when the RSR is directly read, unless the alarm condition still exists. Count-overflow interrupts (those driven by on-board event counters) will be conditionally cleared by reading the RSR; the next event will trigger interrupt unless the user presets the appropriate count register. RSR data may be polled by a burst read, which leaves the contents unaffected.

RIMR: RECEIVE INTERRUPT MASK REGISTER Figure 18

(MSB) (LSB)

BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
BVCS	RIMR.7	**Bipolar Violation Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
ECS	RIMR.6	**Error Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
RYEL	RIMR.5	**Receive Yellow Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
RCL	RIMR.4	**Receive Carrier Loss Mask.** 1 = interrupt enabled 0 = interrupt masked
FERR	RIMR.3	**Frame Bit Error Mask.** 1 = interrupt enabled 0 = interrupt masked
B8ZSD	RIMR.2	**B8ZS Detect Mask.** 1 = interrupt enabled 0 = interrupt masked
RBL	RIMR.1	**Receive Blue Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
RLOS	RIMR.0	**Receive Loss of Sync Mask.** 1 = interrupt enabled 0 = interrupt masked

ALARM COUNTERS

The three on-board alarm event counters allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presettable by the user, establishing an event count interrupt threshold. As each counter saturates, it will set a bit in the RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

OOF EVENTS AND ERRORED SUPERFRAMES

Out of frame is declared when two (or more) of four consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S, the FPS bits are tested in 193E. OOF events are recorded by the 4-bit OOF counter in the error count register. In the 193E framing mode, the OOF event is logically "OR'ed" with an on-chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4-bit ESF error counter in the error count register. In the 193S framing mode, the 4-bit ESF error counter records individual F_T and F_S errors when RCR.3 = 1, or F_T errors only when RCR.3 = 0.

BVCR: BIPOLAR VIOLATION COUNT REGISTER Figure 19

(MSB) (LSB)

BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

SYMBOL	POSITION	NAME AND DESCRIPTION
BVD7	BVCR.7	MSB of bipolar violation count
BVD0	BVCR.0	LSB of bipolar violation count

This 8 bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation once saturated (RIMR.7 = 1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "up" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

ECR: ERROR COUNT REGISTER Figure 20

(MSB) (LSB)

OOFD3	OOFD2	OOFD1	OOFD0	ESFD3	ESFD2	ESFD1	ESFD0
← OOF COUNT →				← ESF ERROR COUNT →			

SYMBOL	POSITION	NAME AND DESCRIPTION
OOFD3	ECR.7	MSB of OOF event count
OOFD0	ECR.4	LSB of OOF event count
ESFD3	ECR.3	MSB of extended superframe error count
ESFD0	ECR.0	LSB of extended superframe error count

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF error event after saturation (RIMR.6 = 1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counters will count "up" to saturation from the preset value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously.

The OOF counter records out-of-frame events in both 193-S and 193E. The ESF error counter records errored superframes in 193E. In 193S the ESF counter records individual F_T and F_S errors when RCR.3 = 1; F_T errors only when RCR.3 = 0. ECR counter increments are disabled when resync is in progress (RLOS high).

ALARM OUTPUTS

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on-board alarm logic.

RLOS OUTPUT

The receive loss of sync output indicates the status of the receiver synchronizer circuitry: when high, an off-line resynchronization is in progress and a high-low transition indicates resync is complete. The RLOS bit (RSR.0) is a "latched" version of the RLOS output. If the auto-resync mode is selected (RCR.1 = 0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RYEL OUTPUT

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR.5) is a "latched" version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 (Hex) and FF (Hex) received at RLINK. In 193S framing the yellow alarm format is dependent on CCR.3: if CCR.3 = 0, the RYEL output transitions high if bit 2 of 256 or more consecutive channels is 0; if CCR.3 = 1, yellow alarm is declared when the S-bit received in frame 12 is 1.

RBV OUTPUT

The bipolar violation output transitions high when accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

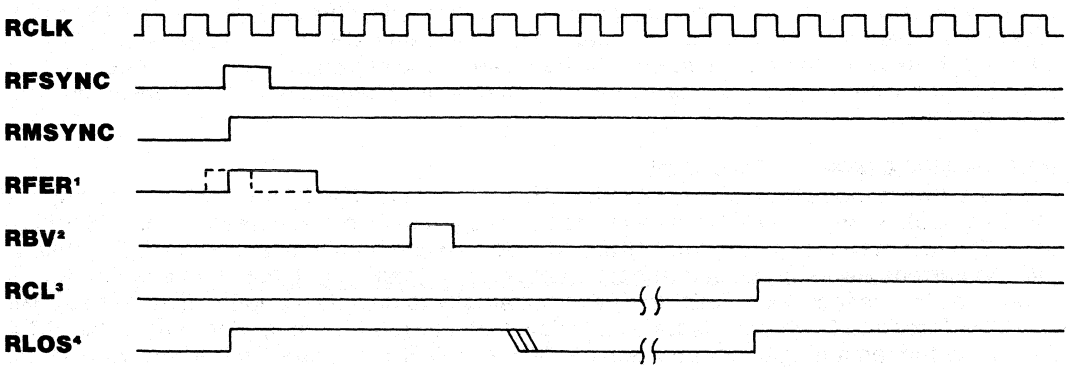
RFER OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S framing F_T and F_S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low-high-low transition (one bit period wide) one half RCLK period before a low-high transition on RMSYNC.

RESET

A high-low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power-up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

ALARM OUTPUT TIMING Figure 21



NOTES:

1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if CCR.3 = 1.) Also, in 193E, RFER transitions ½ bit time before the rising edge of RMSYNC to indicate a CRC error for the previous multiframe.
2. RBV indicates received bipolar violation and transitions high when accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high (during 32nd bit time) when 32 consecutive bits received are "0"; RCL transitions low when the next "1" is received.
4. RLOS transitions high during the F-bit time that caused an OOF event (any 2 of 4 consecutive F_T or FPS bits are in error) if auto-resync mode is selected (RCR.1 = 0). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR.1 = 1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR.0 transitions low-to-high or the RST pin transitions high-low-high.

HARDWARE MODE

For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying SPS to VSS disables the serial port, clears all internal registers except CCR and TCR and redefines pins 14 through 18 as mode control inputs. The hardware mode allows device retrofit into existing applications where mode control and alarm conditioning hardware is often designed with discrete logic.

HARDWARE COMMON CONTROL

In the hardware mode bits TCR.2, CCR.4, TCR.0, CCR.1 and CCR.2 map to pins 14 through 18. The loopback feature (bit CCR.0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched as when both pins are taken high, preserving the current zero suppression mode). Robbed bit signalling (bit TCR.4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. Bit CCR.3 is forced to 0, which selects bit 2 yellow alarm in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in the hardware mode. The $\overline{RST}$ input may be used to force immediate receiver resync, and has no effect on transmit.

HARDWARE MODE Table 6

PIN NUMBER	REGISTER BIT LOCATION	NAME AND DESCRIPTION
14	**TCR-D2**	**193S - S-bit insertion[3].** 1 = external; 0 = internal
15	**CCR-D4**	**Framing Mode Select.** 1 = 193E; 0 = 193S
16	**TCR-D0**	**Transmit Yellow Alarm[2,3].** 1 = enabled; 0 = disabled
17	**CCR-D1**	**Zero Suppression[1].** 1 = bit 7 stuffing 0 = transparent
18	**CCR-D2**	**B8ZS[1].** 1 = enabled; 0 = disabled

NOTES:
1. Tying pins 17 and 18 high enables loopback in the hardware mode.
2. Bit 2 (193S) and data link (193E) yellow alarms are supported.
3. S-bit yellow alarm (193S) is not internally supported; however, the user may elect to insert external S-bits for alarm purposes.

T1 Overview

FRAMING STANDARDS

The DS2180 is compatible with the existing Bell System D4 framing standard described in ATT PUB 43801 and the new extended superframe format (ESF) as described in ATT C.B. #142. In this document, D4 framing is referred to as 193S, and ESF (also known as Fe) is referred to as 193E. Programmable features of the DS2180 allow support of other framing standards which are derivatives of 193E and 193S. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position. In 193S, 12 frames make up a superframe; in 193E, 24. A frame consists of 24 channels (time-slots) of 8-bit data preceded by an F-bit. Channel data is transmitted and received MSB first.

F-BITS

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F_T-bits) which provides frame alignment information, and the signaling framing pattern (known as F_S-bits) which provides multiframe alignment information. In 193E framing, the F-bit position is shared by the framing pattern sequence (FPS), which provides frame and multiframe alignment information, a 4 KHz data link (facility data link) known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK) and the CRC bits are an indicator of link quality and may be monitored by the user to establish error performance.

SIGNALING

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted. In 193E, A and B data is inserted into frames 6 and 12, and C and D data is inserted into frames 18 and 24. This allows a maximum of 4 signaling states to be transmitted per superframe in 193S and 16 states in 193E.

ALARMS

The DS2180 supports all alarm pattern generation and detection required in typical Bell System applications. These alarm modes are explained in ATT PUB 43801, ATT C.B. #142 and elsewhere in this document.

193E FRAMING FORMAT Table 7

FRAME NUMBER	F-BIT USE			BIT USE IN EACH CHANNEL		SIGNALING-BIT USE		
	FPS[1]	FDL[2]	CRC[3]	DATA	SIGNALING[4,5]	2 STATE	4 STATE	16 STATE
1	—	M	—	BITS 1-8				
2	—	—	C1	BITS 1-8				
3	—	M	—	BITS 1-8				
4	0	—	—	BITS 1-8				
5	—	M	—	BITS 1-8				
6	—	—	C2	BITS 1-7	**BIT 8**	A	A	A
7	—	M	—	BITS 1-8				
8	0	—	—	BITS 1-8				
9	—	M	—	BITS 1-8				
10	—	—	C3	BITS 1-8				
11	—	M	—	BITS 1-8				
12	1	—	—	BITS 1-7	**BIT 8**	A	B	B
13	—	M	—	BITS 1-8				
14	—	—	C4	BITS 1-8				
15	—	M	—	BITS 1-8				
16	0	—	—	BITS 1-8				
17	—	M	—	BITS 1-8				
18	—	—	C5	BITS 1-7	**BIT 8**	A	A	C
19	—	M	—	BITS 1-8				
20	1	—	—	BITS 1-8				
21	—	M	—	BITS 1-8				
22	—	—	C6	BITS 1-8				
23	—	M	—	BITS 1-8				
24	1	—	—	BITS 1-7	**BIT 8**	A	B	D

NOTES:

1. FPS - Framing Pattern Sequence.
2. FDL - 4 KHz Facility Data Link; M = message bits.
3. CRC - Cyclic Redundancy Check Bits. The CRC code will be internally generated by the device when TCR.5 = 0. When TCR.5 = 1, externally supplied CRC data will be sampled at TSER during the F-bit time of frames 2, 6, 10, 14, 18, 22.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.
5. Depending on application, the user can support 2-state, 4-state or 16-state signaling by the appropriate decodes of TMO, TSIGFR, TSIGSEL (Transmit Side) and RMSYNC, RSIGFR AND RSIGSEL (Receive Side).

193S FRAMING FORMAT Table 8

FRAME NUMBER	F-BIT USE		BIT USE IN EACH CHANNEL		SIGNALING-BIT USE
	F_T[1]	F_S[2]	DATA	SIGNALING[4]	
1	1	—	BITS 1-8		
2	—	0	BITS 1-8		
3	0	—	BITS 1-8		
4	—	0	BITS 1-8		
5	1	—	BITS 1-8		
6	—	1	BITS 1-7	**BIT 8**	A
7	0	—	BITS 1-8		
8	—	1	BITS 1-8		
9	1	—	BITS 1-8		
10	—	1	BITS 1-8		
11	0	—	BITS 1-8		
12	—	0[3]	BITS 1-7	**BIT 8**	B

NOTES:
1. F_T (terminal framing) bits provide frame alignment information.
2. F_S (signaling frame) bits provide multiframe alignment information.
3. The S-bit in frame 12 may be used for yellow alarm transmission and detection in some applications.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.

LINE CODING

T1 line data is transmitted in a bipolar alternative mark inversion line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit 7 of any channel consisting of all 0's to 1. The use of Bipolar Eight Zero Substitution (B8ZS) satisfies the one's density requirement, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in ATT C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "one" transmitted was positive, the inserted code is 000+ −0− +; if negative, the code word inserted is 000− +0+ −. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the DS2180 error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all 0's if B8ZS is enabled. Also, the receive status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR.2.

Transmit Side Overview

The transmit side of the DS2180 is made up of 6 major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC. The timing and clock generation circuit develops all on-board and output clocks to the system from inputs TCLK, TFSYNC and TMSYNC. The yellow alarm circuitry generates mode dependent yellow alarms. The CRC block generates checksum results utilized in 193E framing. F-bit data provides mode dependent framing patterns and allows insertion of link or S-bit data externally. All of these blocks feed into the data selector, where under control of the CCR, TCR, TIRs and TTRs, the contents of the outgoing data stream are established by bit selection and insertion. The bipolar coder formats the output of the data selector to make it compatible with bipolar transmission techniques and inserts zero suppression codes. The bipolar coder also supports the on-board loopback feature. Input to output delay of the transmitter is 10 TCLK cycles.

Receive Side Overview

SYNCHRONIZER
The heart of the receiver is the synchronizer/sync monitor. This circuit serves two purposes: 1) monitoring the incoming data stream for loss of frame or multiframe alignment, and 2) searching for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR, which is forced low during resync. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR allow tailoring of the resync algorithm by the user. These bits are described below.

SYNC TIME (RCR.2)
Bit RCR.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR.2 = 1, the algorithm will validate 24 bits; if RCR.2 = 0, 10 bits are validated. 24-bit testing results in superior false framing protection, while 10-bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

RESYNC (RCR.0)
A zero-to-one transition of RCR.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

SYNC ENABLE (RCR.1)
When RCR.1 is cleared, the receiver will initiate automatic resync if any of the following events occur: 1) an OOF event ("out-of-frame"), or 2) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR.1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR.0 to 1, or externally via a low-high transition on $\overline{RST}$. Note that using $\overline{RST}$ to initiate resync resets the receive output timing while $\overline{RST}$ is low; use of RCR.1 does not affect output timing until the new alignment is located.

SYNC CRITERIA (RCR.3)

193E

Bit RCR.3 determines which sync algorithm is utilized when resync is in progress (RLOS = 1). In 193E framing, when RCR.3 = 0, the synchronizer will lock only to the FPS pattern and will move to the new frame and multiframe alignment after the framing candidate is qualified. RLOS will go low one frame after the move to the new alignment. When RCR.3 = 1, the new alignment is further tested by a CRC code match. RLOS will transition low after a CRC match occurs. If no CRC match occurs in three attempts (three multiframes), the algorithm will reset and a new search for the framing pattern begins. It takes 9 ms for the synchronizer to check the first CRC code after the new alignment has been loaded. Each additional CRC test takes 3 msec. Regardless of the state of RCR.3, if more than one candidate exists after about 24 milliseconds, the synchronizer will begin eliminating emulators by testing their CRC codes on-line in order to find the true framing candidate.

193S

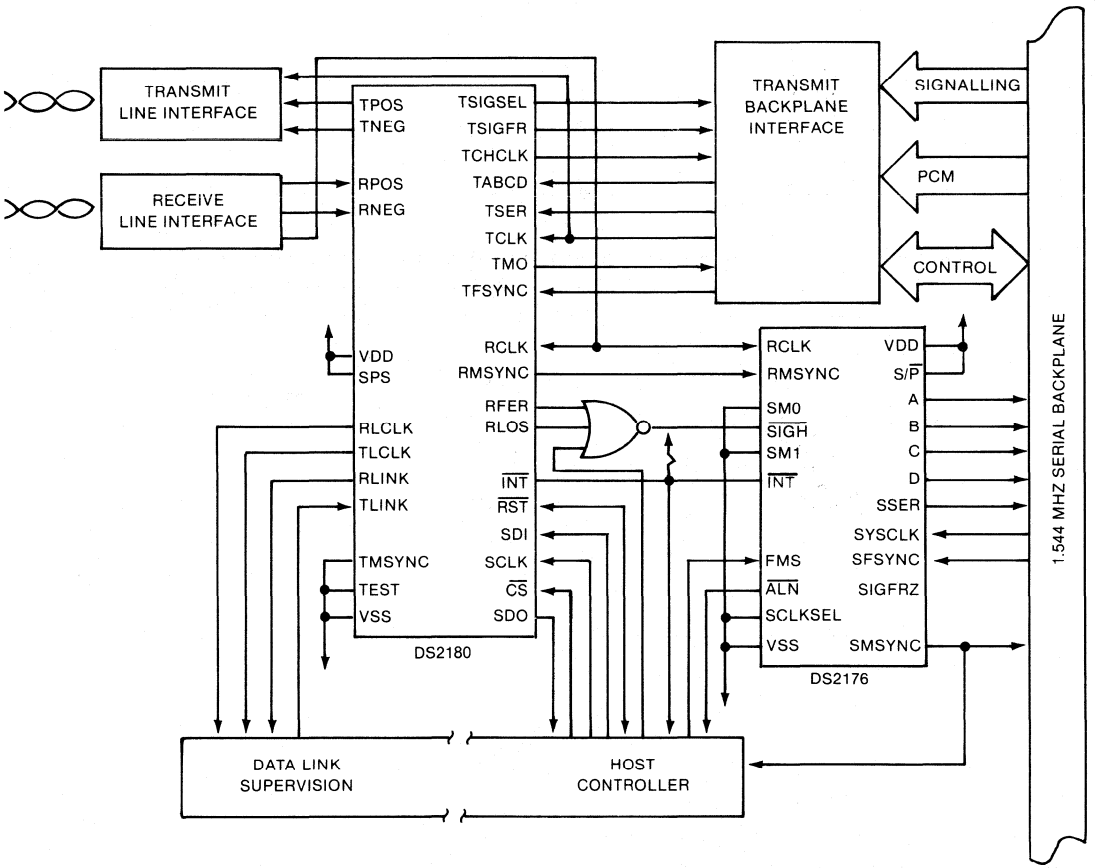
In 193S framing, when RCR.3 = 1, the synchronizer will cross check the F_T pattern with the F_S pattern to help eliminate false framing candidates such as digital milliwatts. The F_S patterns are compared to the repeating pattern . . . 00111000111000 . . . (00111X0 if CCR.3—YELMD—is equal to a 1).In this mode, F_T and F_S patterns must be correctly identified by the synchronizer before sync is declared. Clearing RCR.3 causes the synchronizer to search for F_T patterns (101010 . . .) without cross-coupling the F_S pattern. Frame sync will be established using the F_T information, while multiframe sync will be established only if valid F_S information is present. If no valid F_S pattern is identified, the synchronizer will move to the F_T alignment, RLOS will go low, and a false multiframe position may be indicated by RMSYNC. RFER will indicate when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode will be used in applications where non-standard S-bit patterns exist. In such applications multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

AVERAGE REFRAME TIME[1] Table 9

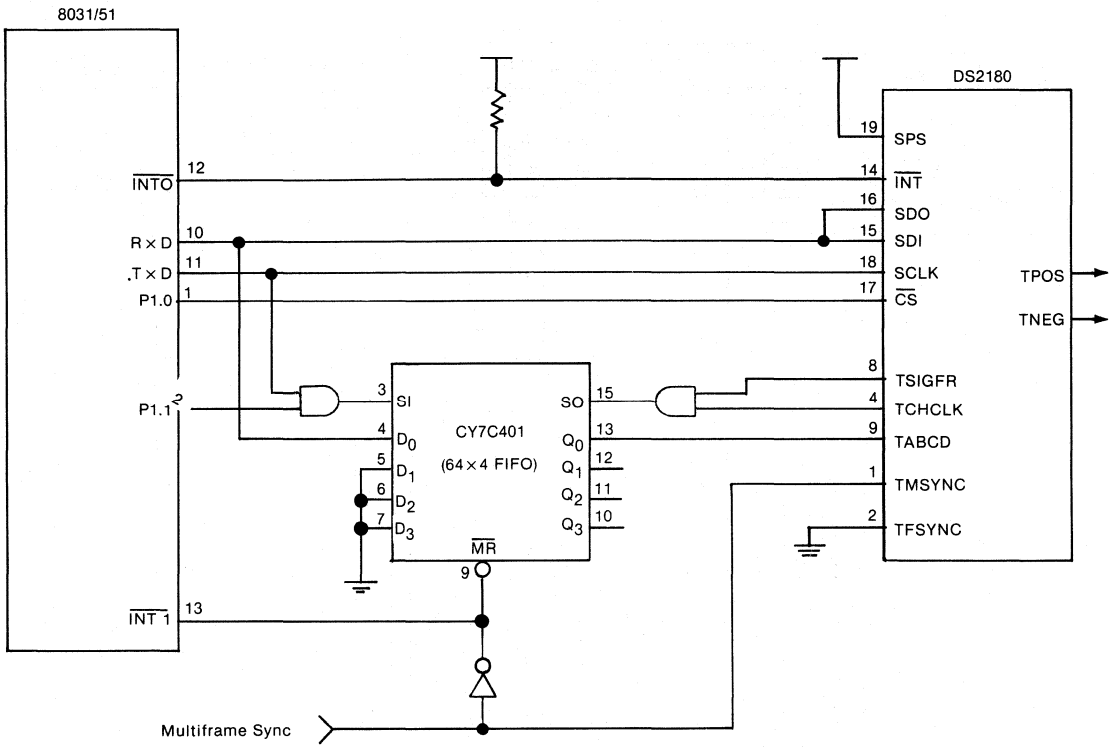
FRAME MODE	RCR.2 = 0			RCR.2 = 1			UNITS
	MIN	AVG	MAX	MIN	AVG	MAX	
193S	3.0	3.75	4.5	6.5	7.25	8.0	msec
193E	6.0	7.5	9.0	13.0	14.5	16.0	

NOTES: 1. Average Reframe Time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

BACKPLANE INTERFACE USING DS2180 AND DS2176 Figure 22



PROCESSOR-BASED TRANSMIT SIGNALLING INSERTION Figure 23



PROCESSOR-BASED SIGNALING

Many robbed-bit signaling applications utilize a microprocessor to insert transmit signaling data into the outgoing data stream. The circuit shown in figure 23 "decouples" the processor timing from that of the DS2180 by use of a small FIFO memory. The processor writes to the FIFO (6 bytes are written: 3 for A data, 3 for B data) only when signaling updates are required. The FIFO automatically retransmits old data when no updates occur. The system is interrupt-driven from the transmit multiframe sync input; the processor must update the FIFO prior to Frame 6 (625 *u*s) after interrupt) to prevent data corruption. The application circuit shown supports 193S framing; additional hardware is required for 193E applications.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to 70°
STORAGE TEMPERATURE	—	−40°C to 70°C
SOLDERING TEMPERATURE	—	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Logic 1	V_{IH}	2.0		V_{DD} + .3	V
Logic 0	V_{IL}	−0.3		+0.8	V
Supply	V_{DD}	4.5	5.0	5.5	V

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	7	pF

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{DD}		3		mA	1,2
Input Leakage	I_{IL}			1	µA	
Output Leakage	I_{LO}			1	µA	3
Output Current @ 2.4V	I_{OH}	−1			mA	4
Output Current @ .4V	I_{OL}			+4	mA	5

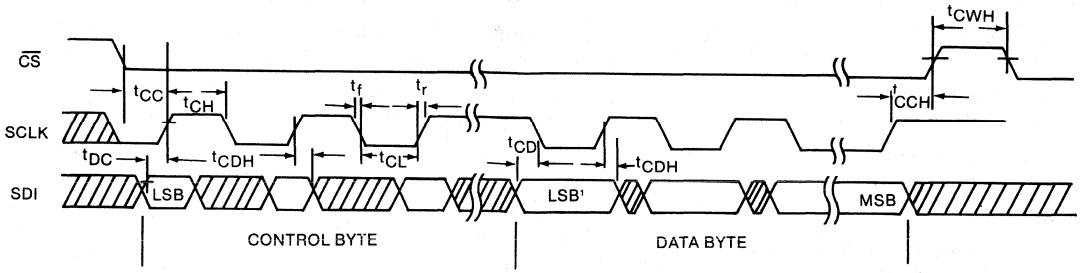
NOTES: 1. TCLK = RCLK = 1.544 MHz
2. Outputs open
3. Applies to SDO when tristated
4. All outputs except $\overline{INT}$, which is open collector
5. All outputs

A.C. ELECTRICAL CHARACTERISTICS[1] — SERIAL PORT (0 °C to 70 ° V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
SDI to SCLK Set up	t_{DC}	50			ns
SCLK to SDI Hold	t_{CDH}	50			ns
SDI to SCLK Falling Edge	t_{CD}	50			ns
SCLK Low Time	t_{CL}	250			ns
SCLK High Time	t_{CH}	250			ns
SCLK Rise & Fall Time	t_R, t_F			500	ns
$\overline{CS}$ to SCLK Set Up	t_{CC}	50			ns
SCLK to $\overline{CS}$ Hold	t_{CCH}	50			ns
$\overline{CS}$ Inactive Time	t_{CWH}	250			ns
SCLK to SDO Valid[2]	t_{CDV}			200	ns
$\overline{CS}$ to SDO High Z	t_{CDZ}			75	ns

NOTES: 1.Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
2.Output load capacitance = 100 pF.

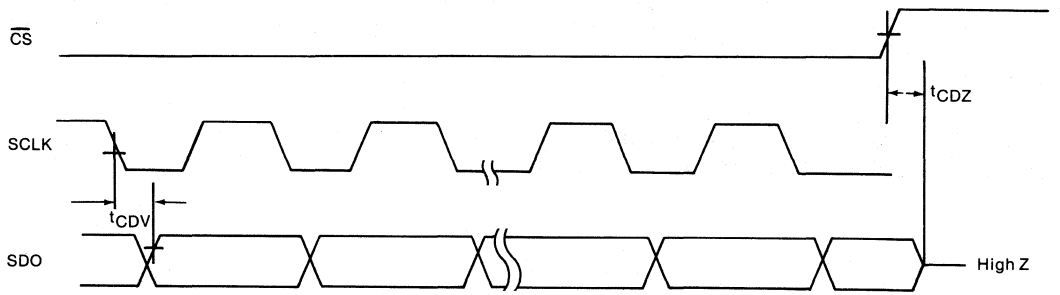
SERIAL PORT WRITE A.C. TIMING DIAGRAM



NOTES: 1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.

2. Shaded regions indicate don't-care states of input data.

SERIAL PORT READ[1] A.C. TIMING



NOTES: 1. Serial port write must precede a port read to provide address information.

A.C. ELECTRICAL CHARACTERISTICS[1] — TRANSMIT (0 °C to 70°, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
TCLK Period	t_P		648		ns
TCLK Pulse Width	t_{WL}, t_{WH}		324		ns
TCLK, RCLK Rise & Fall Times	t_F, t_R		20		ns
TSER, TABCD, TLINK Set Up to TCLK Falling	t_{STD}	50			ns
TSER, TABCD,TLINK Hold to TCLK Falling	t_{HTD}	50			ns
TFSYNC, TMSYNC Set Up to TCLK Rising	t_{STS}	– 125		125	ns
Propagation Delay TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}			75	ns
Propagation Delay TCLK to TCHCLK	t_{PTCH}			75	ns
TFSYNC, TMSYNC Pulse Width	t_{TSP}	100			ns

NOTES:

1.Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
2.Output load capacitance = 100 pF.

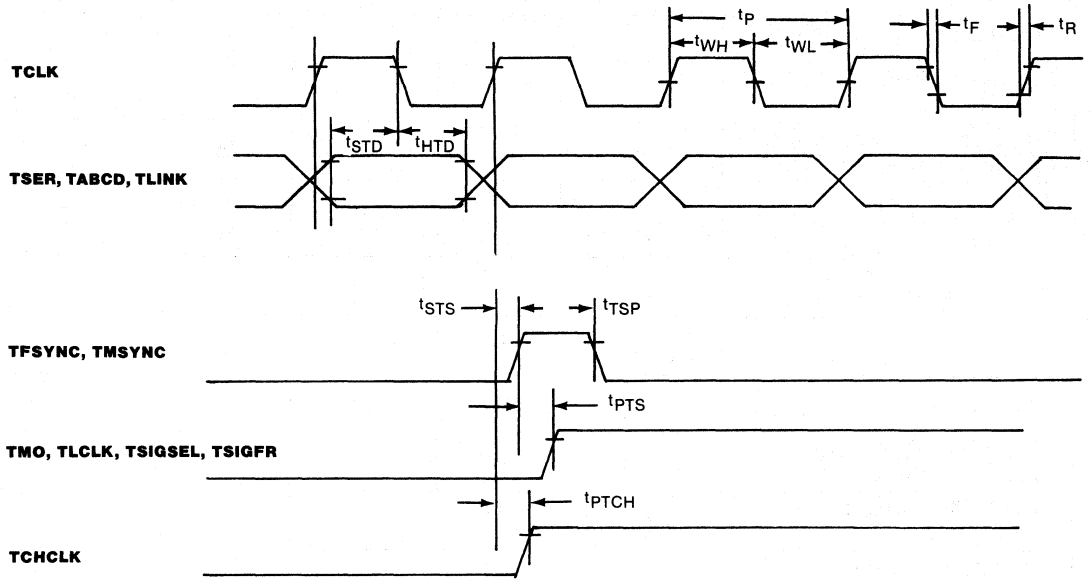
A.C. ELECTRICAL CHARACTERISTICS[1] — RECEIVE (0 °C to 70 °, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Propagation Delay RCLK to RMSYNC, RFSYNC, RSIGSEL, RSIGFR, RLCLK, RCHCLK	t_{PRS}			75	ns
Propagation Delay RCLK to RSER, RABCD, RLINK	t_{PRD}			75	ns
Transition Time All Outputs	t_{TTR}			20	ns
RCLK Period	t_P		648		ns
RCLK Pulse Width	t_{WL}, t_{WH}	124	324	524	ns
RCLK Rise & Fall Times	t_R, t_F		20		ns
RPOS, RNEG Set Up to RCLK Falling	t_{SRD}	50			ns
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns
Propagation Delay RCLK to RYEL, RCL, RFER, RLOS, RBV	t_{PRA}			75	ns
Minimum RST Pulse Width on System Power Up or Restart	t_{RST}	100			ns

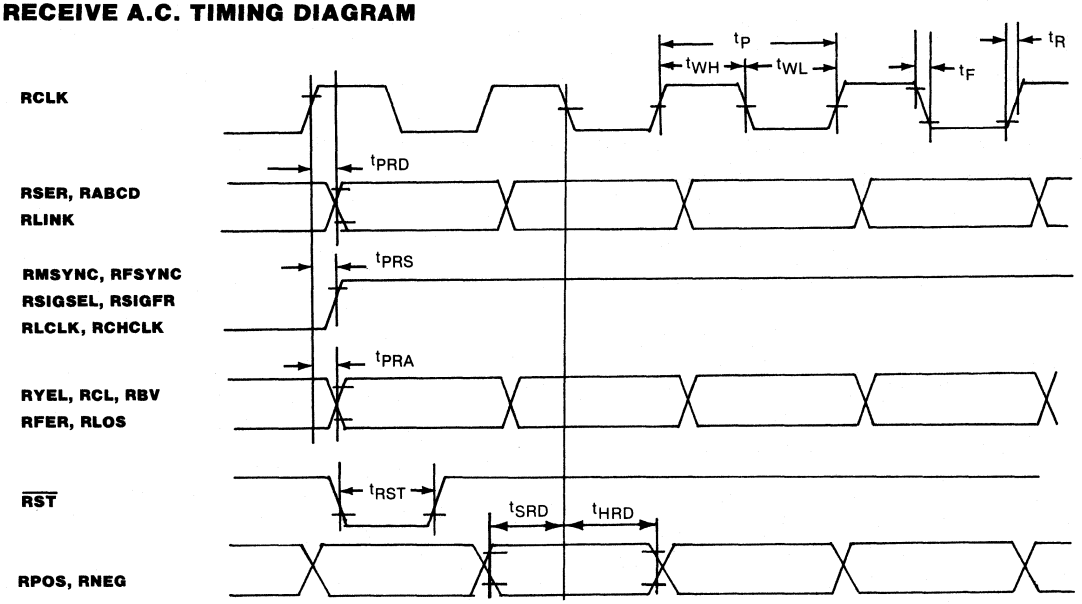
NOTES:

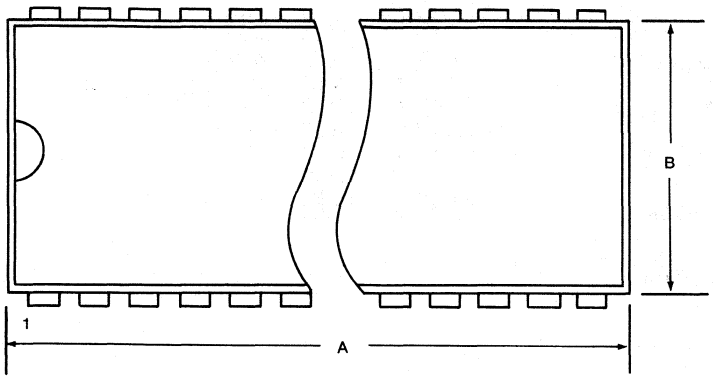
1.Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
2.Output load capacitance = 100 pF.

TRANSMIT A.C. TIMING DIAGRAM

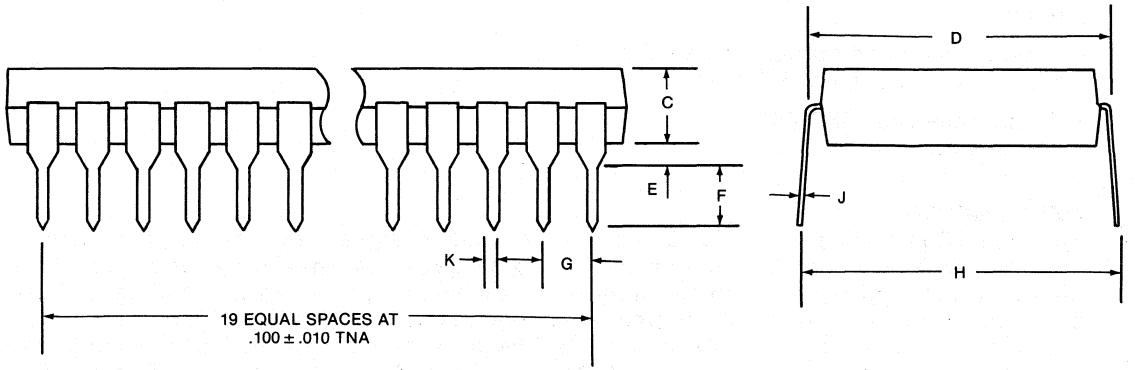


RECEIVE A.C. TIMING DIAGRAM





DIM.	INCHES	
	MIN.	MAX.
A	2.040	2.080
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021



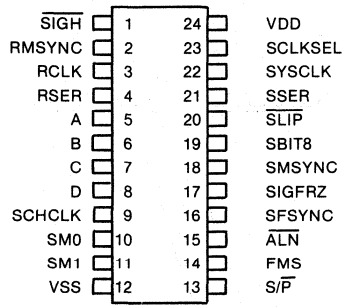
Dallas Semiconductor
T1 Receive Buffer

PRELIMINARY
DS2176

FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180 T1 Transceiver

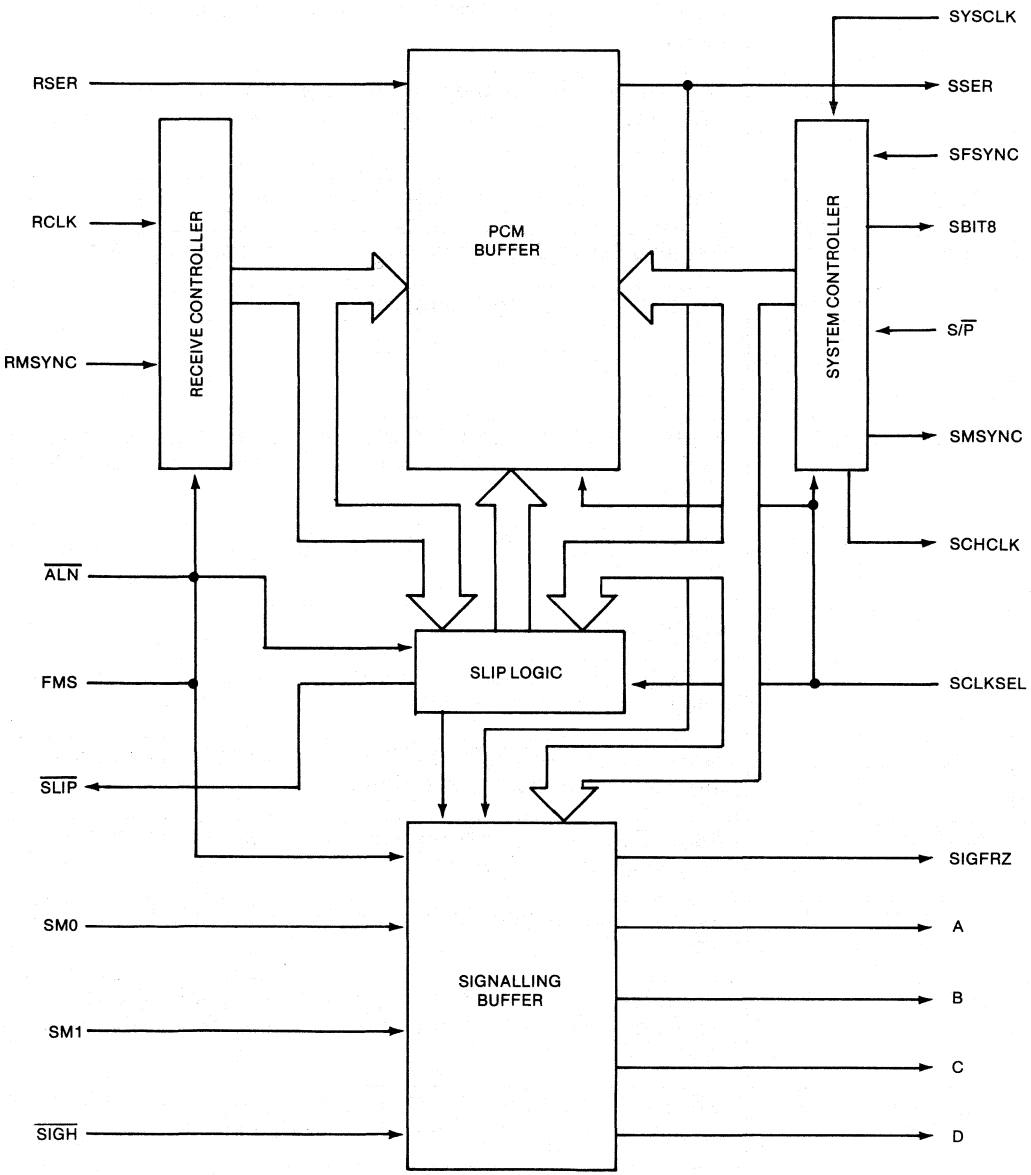
PIN CONNECTIONS



DESCRIPTION

The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2176 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

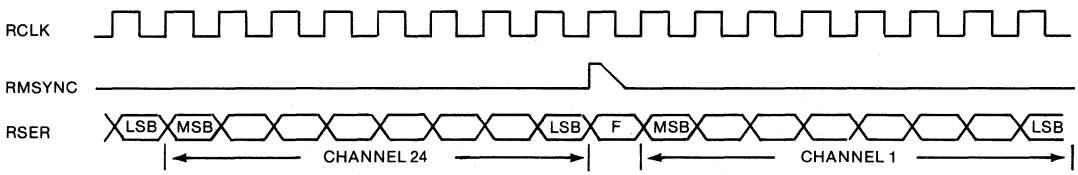
PIN	SYMBOL	TYPE	DESCRIPTION
1	$\overline{\text{SIGH}}$	I	**Signalling Inhibit.** When low, ABCD signalling updates are disabled for a period determined by SM0 and SM1, or until returned high.
2	RMSYNC	I	**Receive Multiframe Sync.** Must be pulsed high at multiframe boundaries to establish frame and multiframe alignment.
3	RCLK	I	**Receive Clock.** Primary 1.544 MHz clock.
4	RSER	I	**Receive Serial Data.** Sampled on falling edge of RCLK.
5 6 7 8	A B C D	O	**Robbed-Bit Signalling Outputs**
9	SCHCLK	O	**System Channel Clock.** Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
10 11	SM0 SM1	I	**Signalling Modes 0 and 1.** Select signalling supervision technique.
12	VSS	—	**Signal ground.** 0.0 volts.
13	S/$\overline{\text{P}}$	I	**Serial/Parallel Select.** Tie to VSS for parallel backplane applications, to VDD for serial.
14	FMS	I	**Frame Mode Select.** Tie to VSS to select 193S (D4) framing, to VDD for 193E (extended).
15	$\overline{\text{ALN}}$	I	**Align.** Recenters buffer on next system side frame boundary when forced low.
16	SFSYNC	I	**System Frame Sync.** Rising edge establishes start of frame.
17	SIGFRZ	I	**Signalling Freeze.** When high, indicates signalling updates have been disabled internally via a slip or externally by forcing $\overline{\text{SIGH}}$ low.
18	SMSYNC	O	**System Multiframe Sync.** Slip-compensated multiframe output; indicates when signalling updates are made.
19	SBIT8	O	**System Bit 8.** High during the LSB time of each channel. Used to reinsert extracted signalling into outgoing data stream.

20	$\overline{\text{SLIP}}$	O	**Frame Slip.** Active low, open collector output. Held low for 64 SYSCLK cycles when a slip occurs.
21	SSER	O	**System Serial Out.** Updated on rising edge of SYSCLK.
22	SYSCLK	I	**System Clock.** 1.544 or 2.048 MHz data clock.
23	SCLKSEL	I	**System Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
24	VDD	—	**Positive Supply.** 5.0 volts.

OVERVIEW

The DS2176 performs two primary functions: 1) *synchronization* of received T1 PCM data (looped timed) to host backplane frequencies; 2) *supervision* of robbed-bit signalling data embedded in the data stream. The buffer, while optimized for use with the DS2180 T1 Transceiver, is also compatible with other transceiver devices. The DS2180 data sheet should serve as a valuable reference when designing with the DS2176.

RECEIVE SIDE TIMING Figure 2



DATA SYNCHRONIZATION

PCM BUFFER

The DS2176 utilizes a 2-frame buffer (386 bits) to synchronize incoming PCM data to the system backplane clock. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. A rising edge at RMSYNC establishes receive side frame and multiframe alignment. A rising edge at SFSYNC establishes system side frame alignment. The buffer depth is constantly monitored by on-board contention logic, a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

SLIP CORRECTION CAPABILITY

The 2-frame buffer depth is adequate for most T-carrier applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2176 provides an ideal balance between total delay and slip correction capability.

BUFFER RECENTERING

$\overline{SLIP}$ is held low for 64 SYSCLK cycles when a slip occurs. $\overline{SLIP}$ is an active-low, open-collector output.

BUFFER DEPTH MONITORING

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC real time.

CLOCK SELECT

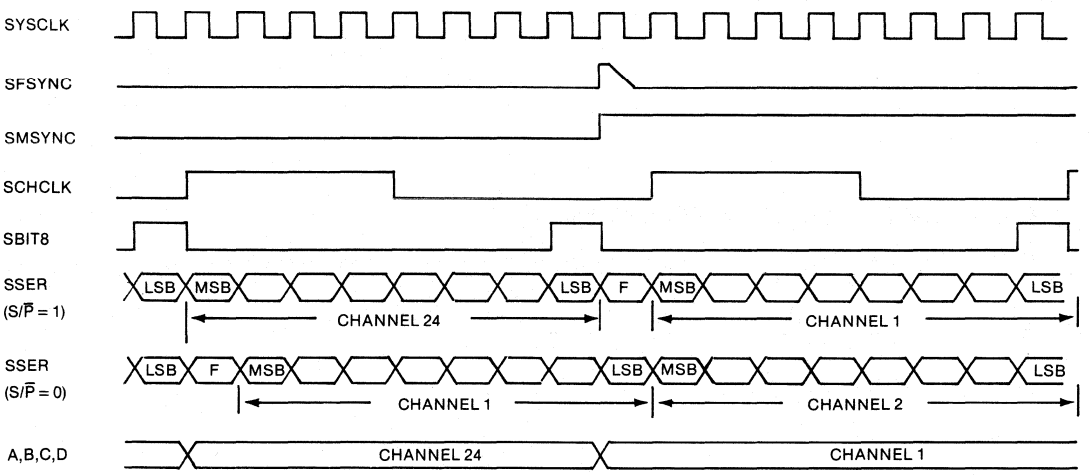
The device is compatible with 2 common backplane frequencies: 1.544 MHz, selected when SCLKSEL = 0; and 2.048 MHz, selected when SCLKSEL = 1. In 1.544 MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is dropped in 2.048 MHz applications and the MSB of channel 1 appears at SSER one bit period after a rising edge at SFSYNC. SSER is forced to 1 in all channels greater than 24. See figures 3 and 4.

In 2.048 MHz applications (SCLKSEL = 1), the PCM buffer control logic establishes slip criteria different from that used in 1.544 MHz applications to compensate for the faster system-side read frequency.

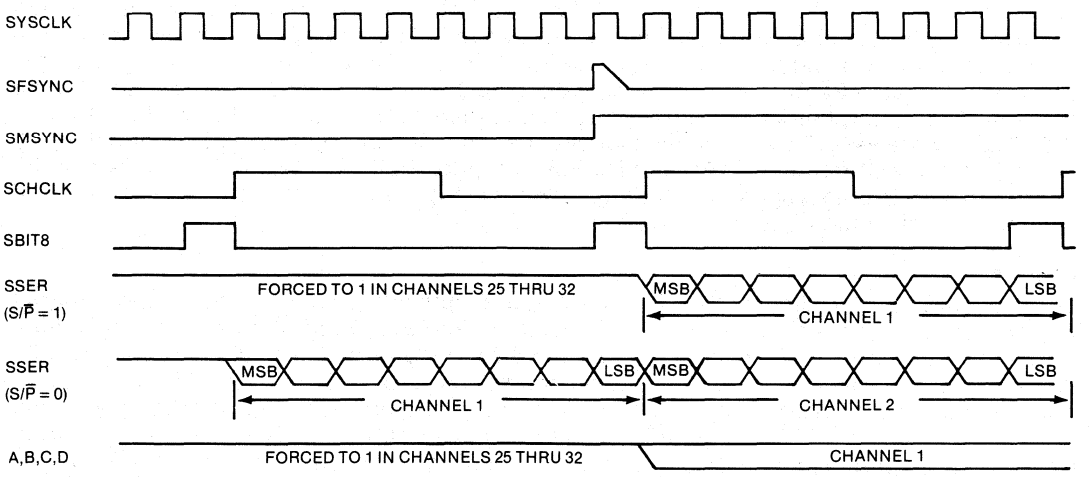
PARALLEL COMPATIBILITY

The DS2176 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC as shown in figures 3 and 4 (serial applications, S/$\overline{P}$ = 1). The device utilizes a look-ahead circuit in parallel applications (S/$\overline{P}$ = 0). Data is output 8 clocks earlier, allowing the user to parallel convert data externally.

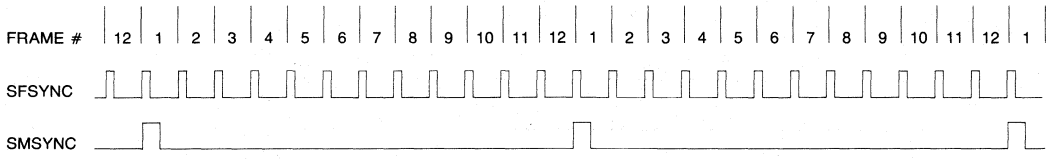
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHZ) Figure 3



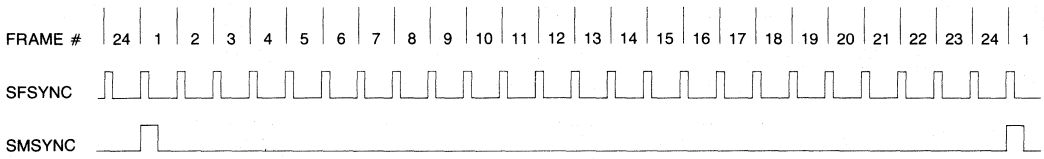
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHZ) Figure 4



193S SYSTEM MULTIFRAME TIMING Figure 5



193E SYSTEM MULTIFRAME TIMING Figure 6



SIGNALLING SUPERVISION

EXTRACTION

In digital channel backs, robbed-bit signalling data is inserted into the LSB position of each channel during signalling frames. In 193S framing (FMS = 0) applications, A signalling data is inserted into frame 6 and B signalling data is inserted into frame 12. 193E framing (FMS = 1) includes 2 additional signalling bits: C signalling is inserted into frame 18 and D signalling is inserted into frame 24. This embedded signalling data is synchronized to system side timing (via the PCM buffer) before being extracted and presented at outputs A,B,C and D. Outputs A,B,C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframe. In 193S applications, outputs C and D contain the previous multiframe's A and B data. Signalling updates occur once per multiframe at the rising edge of SMSYNC unless prohibited by a freeze.

FREEZE

The signalling buffer allows the DS2176 to "freeze" (prevent update of) signalling information during alarm or slip conditions. A slip condition or forcing $\overline{\text{SIGH}}$ low freezes signalling; duration of the freeze is dependent on SM0 and SM1. Updates will be unconditionally prohibited when $\overline{\text{SIGH}}$ is held low. During freezing conditions "old" data is recirculated in the output registers and appears at A,B,C and D. SIGFRZ is held high during the freeze condition, and returns low on the next signalling update. Input to output delay of signalling data is equal to 1 multiframe (the depth of the signalling buffer) + the current depth of the PCM buffer (1 frame ± approximately 1 frame).

INTEGRATION

Signalling integration is another feature of the DS2176; when selected, it minimizes the impact of random noise hits on the span and resultant robbed-bit signalling corruption. Integration requires that per-channel signalling data be in the same state for 2 or more multiframes before appearing at A,B,C and D. SM0 and SM1 are used to select the degree of integration or to totally bypass the feature. Integration is limited to 2 multiframes during slip or alarm conditions to minimize update delay.

CLEAR CHANNEL CONSIDERATIONS

The DS2176 does not merge the "processed" signalling information with outgoing PCM data at SSER; this assures integrity of data in clear channel applications. SBIT8 indicates the LSB position of each channel; when combined with off-chip support logic, it allows the user to selectively re-insert robbed-bit signalling data into the outgoing data stream.

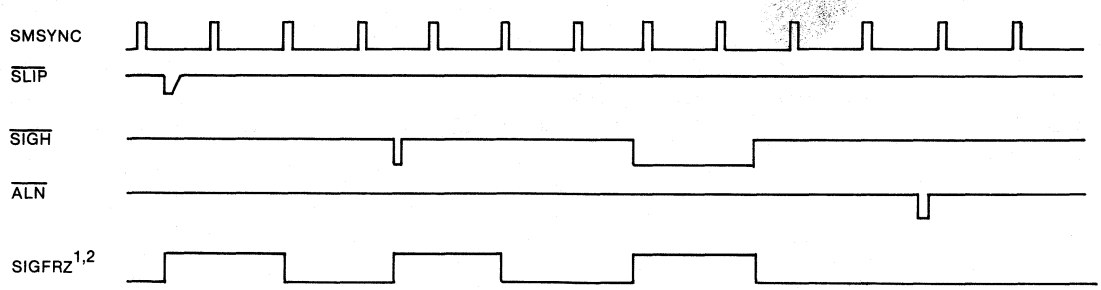
SIGNALLING SUPERVISION MODES Table 2

SM0	SM1	FMS	SELECTED MODE
0	0	0	193S framing, no integration, 1 multiframe freeze.
0	0	1	193E framing, no integration, 1 multiframe freeze.
0	1	0	193S framing, 2 multiframes integration and freeze.
0	1	1	193E framing, 2 multiframes integration and freeze.
1	0	0[1]	193S framing, 5 multiframes integration, 2 multiframes freeze.
1	0	1[1]	193E framing, 3 multiframes integration, 2 multiframes freeze.
1	1	0	Test mode.
1	1	1	Test mode.

NOTES:

1. During slip or alarm conditions, integration is limited to 2 multiframes to minimize signalling delay.

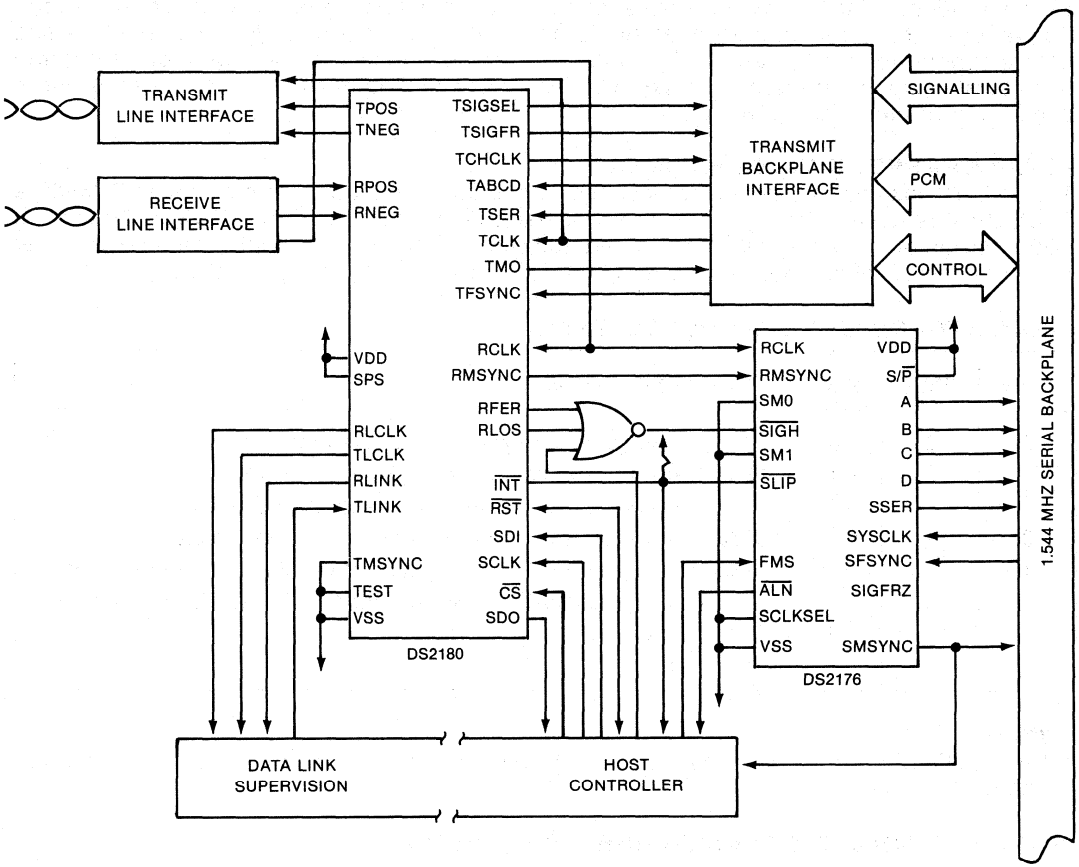
SLIP AND SIGNALLING SUPERVISION LOGIC TIMING Figure 7



NOTES:

1. Integration feature disabled (SM0 = SM1 = 0) in timing set shown.
2. Depending on present buffer depth, forcing $\overline{\text{ALN}}$ low may or may not cause a slip condition.

SERIAL 1.544 MHZ BACKPLANE INTERFACE Figure 8



DS2176/DS2180 SYSTEM APPLICATION
Figure 8 shows how the DS2180 T1 Transceiver and DS2176 Receive Buffer interconnect in a typical application.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V	
Logic 0	V_{IL}	−0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C $V_{DD}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		10		mA	1,2
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	3
Output Current @0.4V	I_{OL}			+4.0	mA	4
Output Leakage	I_{LO}	−1.0		+1.0	uA	5

NOTES:

1. TCLK = RCLK = 1.544 MHz
2. Outputs open
3. All outputs except $\overline{SLIP}$, which is open collector
4. All outputs
5. Applies to $\overline{INT}$ when tri-stated

CAPACITANCE ($t_A = 25°C$)

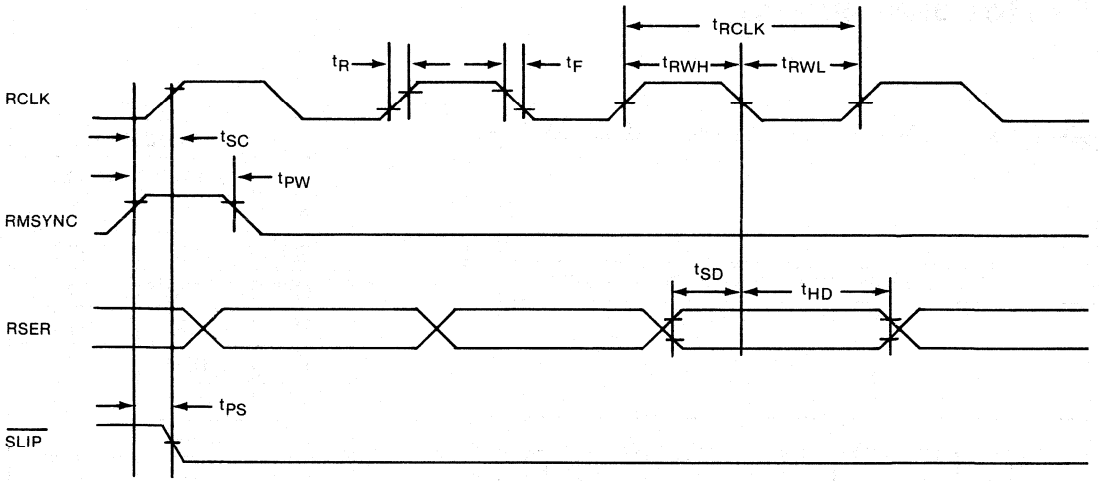
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{DD} = 5V \pm 10\%$)

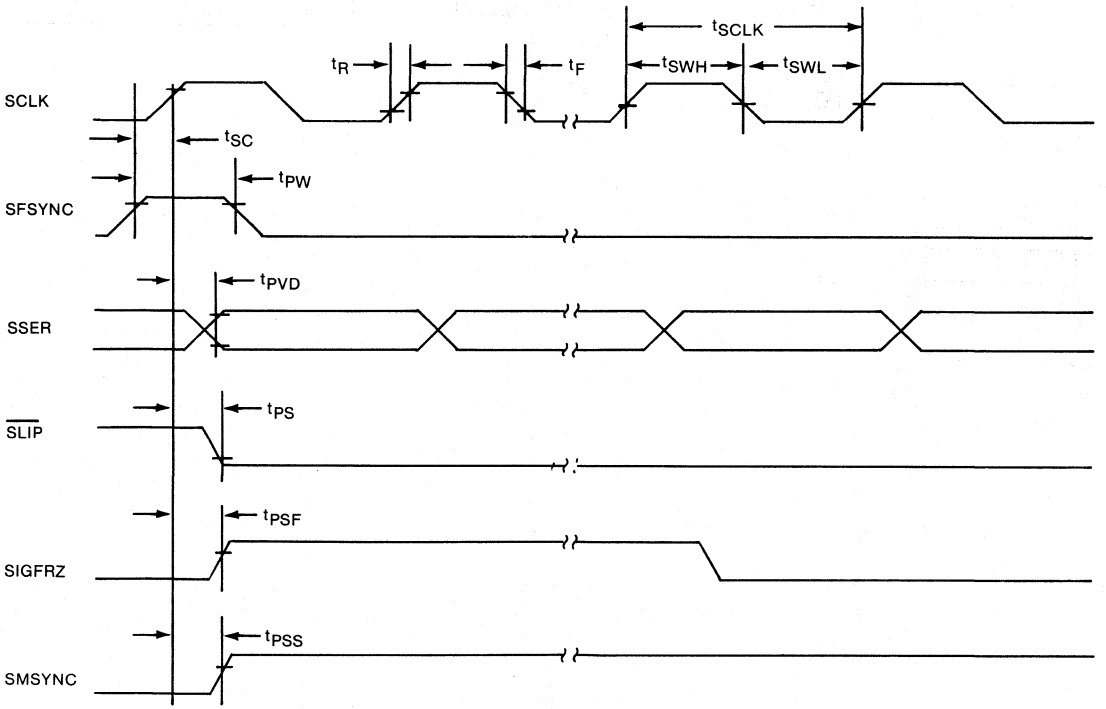
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}		648		ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH}, t_{RWL}		324		ns	
SYSCLK Pulse Width	t_{SWH}, t_{SWL}		244		ns	1
SYSCLK Period	t_{SYSCLK}		488		ns	
RMSYNC, SFSYNC Setup to RCLK, SYSCLK Rising	t_{SC}	-125		+125	ns	
RMSYNC, SFSYNC, $\overline{SIGH}$ $\overline{ALN}$ Pulse Width	t_{PW}	100			ns	
RSER Setup to RCLK Falling	t_{SD}	50			ns	
RSER Hold to RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to SSER, A,B,C,D	t_{PVD}			75	ns	
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low	t_{PS}			100	ns	2,3
Propagation Delay SYSCLK to SIGFRZ Low/High	t_{PSF}			75	ns	
$\overline{ALN}$, $\overline{SIGH}$ Setup to SFSYNC Rising	t_{SR}	500			ns	
$\overline{SIGH}$ Setup to SFSYNC Rising	t_{SR}	500			ns	4

NOTES:
1. SYSCLK = 2.048 MHz
2. At slip occurrence
3. $\overline{SLIP}$ goes out of high impedance
4. $\overline{SIGH}$ with respect to first frame of multiframe (SMSYNC rising)

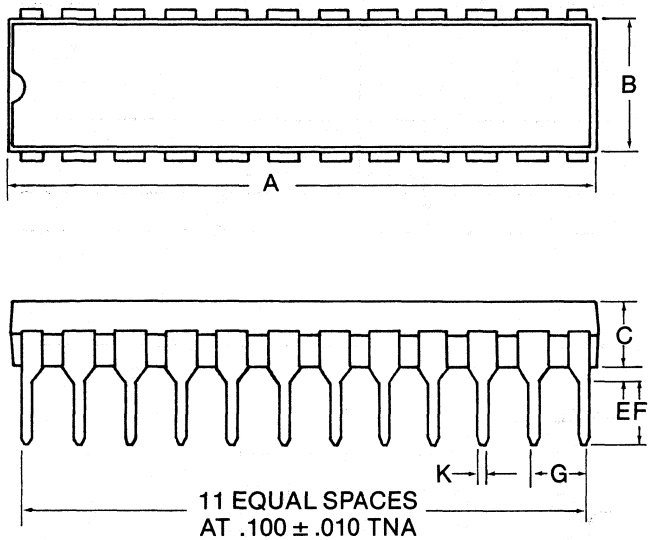
RECEIVE A.C. DIAGRAM Figure 9

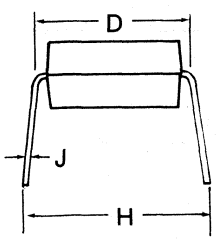


SYSTEM A.C. TIMING DIAGRAM Figure 10



DS2176
T1 Receive Buffer





DIM.	INCHES	
	MIN.	MAX.
A	1.150	1.190
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.325	.375
J	.008	.012
K	.015	.021

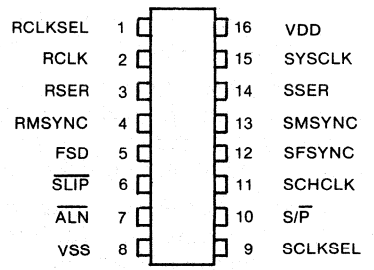
Dallas Semiconductor
T1/CEPT Elastic Store

PRELIMINARY
DS2175

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system-timed data streams
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on-chip "slip" control logic
  - Slips occur only on frame boundaries
  - Output reports slip occurrences
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180 T1 Transceiver

PIN CONNECTIONS



DESCRIPTION

The DS2175 is a low-power CMOS, elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross-connects (DACs), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

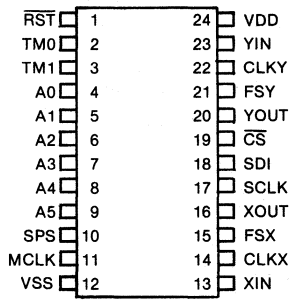
Dallas Semiconductor
ADPCM Processor

PRELIMINARY
DS2168

FEATURES

- PCM compressor/ADPCM expander for use in telecommunications equipment
- Single-chip solution; eliminates general purpose DSP circuits and support logic presently required to perform ADPCM voice encoding and decoding
- Single-channel architecture—device may be programmed to perform full duplex, 2-channel compressions, or 2-channel expansions
- Supports ESCA and CCITT algorithms
- Operates on *u*-law and A-law data
- Serial PCM interface and on-board channel counters compatible with popular combo codecs
- Interfaces to synchronous and asynchronous data streams
- Serial port mode allows single host controller to supervise multiple devices
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Compatible with DS2180 T1 Transceiver
- 5-volt supply, low-power CMOS technology

PIN CONNECTIONS



DESCRIPTION

The DS2168 is a dedicated digital signal processing chip designed for use in applications requiring transcoding between PCM and ADPCM. North American (ESCA) and European (CCITT) algorithms are supported by the device. The circuit contains three major functional blocks; a very high speed DSP engine optimized for the above algorithms, 2 PCM data interfaces which simplify connection to PCM backplanes, and a microprocessor/microcontroller-compatible serial port for device configuration and control. On-chip channel counters eliminate discrete channel-select logic; a bypass feature supports applications which require dynamic allocation of channel bandwidth. A unique addressing scheme allows control port wiring to be shared between multiple devices, minimizing interconnect in transcoder applications. Combo-codec based stand-alone applications are supported by a hardware-control mode.

COMBINED TECHNOLOGIES

Dallas Semiconductor has pioneered three "Late Definition" technologies, creating products with significant applications advantages. By combining low leakage CMOS with either embedded lithium, direct laser writing, or high energy ion implantation, we are able to tailor our products to provide the optimum system solution for each end user.

Through unique applications of our late definition technologies, product innovation has been focused upon solving system problems in these areas:

Nonvolatile SRAMs
Intelligent Sockets
Silicon Timed Circuits
User Insertable Memory
Integrated Battery Back-up
Software Authorization
Telecommunications
System Extension

The following two sections are included as detailed examples of how Late-Definition technologies have been combined with proven CMOS processing to extend the capabilities of IC technology beyond previous limits. Although each section focuses upon one specific product line, the manufacturing flows and test methodologies covered are applicable to other product areas as well. Product development has been accelerated by focusing engineering characterization and reliability studies on a few products chosen as "technology flagships." Engineering work on subsequent products is then able to concentrate upon the key differences of the design or process.

Technology

NONVOLATILE SRAM DETAIL

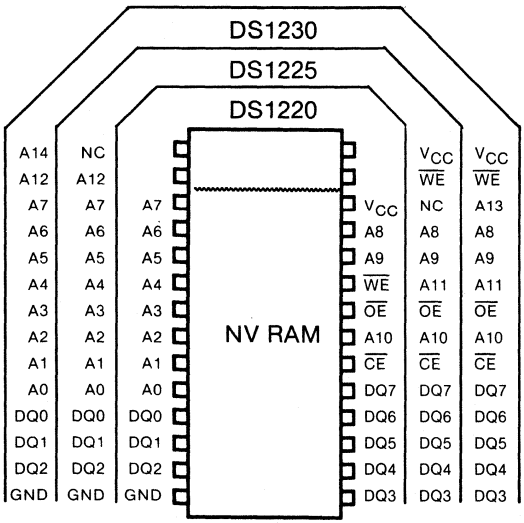
INTRODUCTION AND PRODUCT DESCRIPTION

The DS1220, 1225 & 1230 are fully static nonvolatile RAMs (organized as 2K × 8, 8K × 8, and 32K × 8 respectively) which combine low power CMOS and lithium technologies. Each NV RAM contains a CMOS RAM, a lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition.

These parts provide the ideal solution to nonvolatile memory storage. Normal read and write operations are identical to standard static RAMs. There are no long write cycle requirements as in EEPROMs. No restrictions exist on the number of write cycles and no endurance problems are imposed by charge-trapping in thin oxide layers.

PIN CONNECTIONS

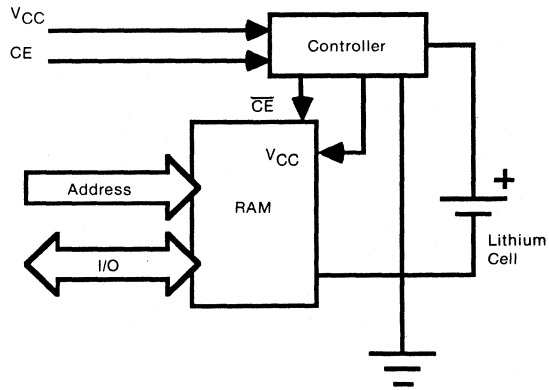
BYTEWIDE JEDEC PINOUT Figure 1



The pinout for each device follows the established industry standard (Figure 1). The Joint Electronic Devices Engineering Council's (JEDEC) Bytewide Version B Standard defines and upgrades from 2K × 8 in density to 32K × 8. This standard accommodates RAMs, ROMs, UV EPROMs and EEPROMs. Because of the flexibility and upgradeability of Bytewide memories, the number of existing sockets is in the hundreds of millions. Therefore many system designs can accommodate direct replacement of RAMs, EPROMs, ROMs and EEPROMs with the DS1220 series of products. These new solutions add real time programmability and/or density upgrades to existing systems without redesign. Real time programmability gives the system the ability to be personalized by the end user.

Each DS1220, 1225 and 1230 integrates a CMOS RAM, a lithium button cell and a VLSI controller chip into a single package as shown in Figure 2.

BLOCK DIAGRAM OF NVRAM Figure 2



The heart of the NV RAM is the intelligent control circuit designed by Dallas Semiconductor to perform the circuit functions required to back up a CMOS memory. First, a switch is provided to direct power from the lithium cell or V_{CC} supply, depending on which is greater. The second function is power fail detection. The controller constantly monitors the V_{CC} supply. If V_{CC} falls below the write protect trip point, V_{tp} (typically 4.25V), a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable to the memory to within 0.2V of V_{CC} or the lithium cell voltage. If the chip enable signal

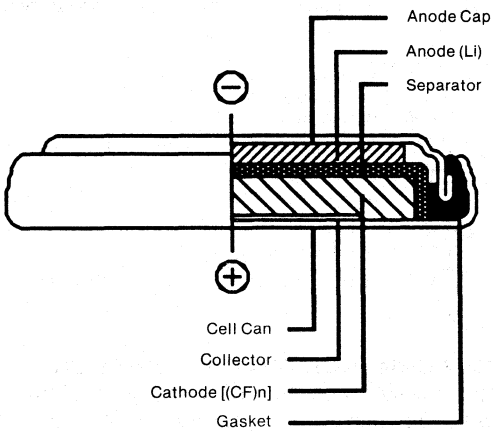
is active at the time power fail detection occurs, write protection id delayed until after the memory cycle is complete to avoid data corruption. During nominal power supply conditions the memory chip enable signal is passed through to the RAM with a typical propagation delay of 10 ns.

DESCRIPTION OF LITHIUM TECHNOLOGY

The energy source used within each NV RAM is a lithium button cell (Type BR1225) measuring 2.5 mm high and 12.5 mm in diameter. Lithium is the lightest metal and also has the highest electrode potential providing very high energy density and a nominal output voltage of 3 volts, about twice that of conventional batteries.

As shown in Figure 3, lithium is used as the anode. It is cut and pressed into a stainless steel cap. The cathode is polycarbonmonofluoride, (CF)n, a solid material chosen for its chemical stability. Polypropylene is used as a separator between the anode and cathode and is saturated in an organic nonaqueous electrolyte.

BR1225 CUTAWAY VIEW Figure 3

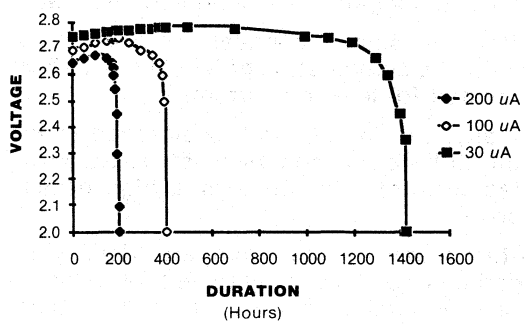


This electro-chemistry is ideal for memory back-up applications because of its high voltage, wide temperature range, high energy density, safety and long shelf life.

The BR1225 cell has a nominal capacity of 38 mAh. The initial open circuit voltage ranges from 3.5V to 3.2V. As shown is Figure 4, lithium cells are noted for their flat discharge characteristics, holding a constant output voltage until the stored energy approaches exhaustion, at which time the output quickly falls to below 2V.

Load characteristic plots such as Figure 4 are used to determine the cell capacity by simply calculating the average output current and multiplying by the time until failure (output 2V). It should be noted that under the very light loads of the NV RAM family (100 nA) the lithium output voltage remains above 3V throughout the lifetime of the cell. Load curves involving such light currents are seldom plotted, however, because of the long time involved in taking such capacity measurements. (Cell lifetime calculations at these loads will be covered later in this report.)

BR1225 DISCHARGE CHARACTERISTICS FOR VARIOUS LOADS Figure 4



PROCESS FLOW DESCRIPTION

Figure 5 illustrates a simplified diagram of the NV RAM series process flow. Each component is carefully screened and tested before assembly into the final product.

The intelligent controller chip (called the DS1218) is first processed and assembled into an 8-pin, 300-mil DIP. Each DS1218 is tested for full functionality and leakage before and after a 12-hour, high temperature

burn-in. The high stress conditions during burn-in accelerate the failure mechanisms induced by latent defects, thus screening out infant mortality failures from the production flow. In order to maximize the data retention lifetime of the completed unit, the controller chip is tested for a maximum DC leakage of 5 nA at 5.75 volts and 25°C.

Each CMOS RAM is burned-in at 125°C and fully tested as part of the Dallas Semiconductor quality assurance program. At Dallas Semiconductor, a 100% functionality and leakage test is repeated with a leakage spec. of 10 nA, at 5.75 volts and 25°C.

Each lithium cell is 100% tested for open circuit voltage and short circuit current, then burned-in for a minimum of two days at 43°C, then 100% retested as before.

Special care is taken in the assembly and test flow to assure maximum data retention lifetime. Figure 6 illustrates the NV RAM assembly in more detail.

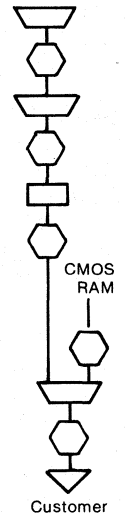
First, a DS1218, a RAM and the lead frame assembly are attached to the interconnect board and vapor phase soldered into place.

After all solder connections have been made, the combination of DS1218 and SRAM is tested for leakage current.

Finally, the lithium cell is attached to the unit and the finished assembly is encapsulated in a plastic tub with a high density epoxy.

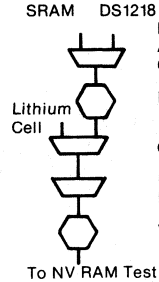
After assembly, all units are visually inspected and electrically tested for full functionality, timing, and lithium cell voltage. The cell voltage specification is 3.2 to 3.5 volts. Functional testing includes data retention and all timing measurements are guardbanded and derated for temperature.

SIMPLIFIED PROCESS FLOW Figure 5



FLOW	PROCESS	FREQUENCY	PARAMETERS
	DS1218 Controller Wafer Fabrication		
	Wafer Sort	100%	Functionality, Leakage
	Assembly & Brand		
	1st Electrical Test	100%	Functionality, Leakage
	Burn-in	100%	12 hrs, 7 volts, 125°C
	2nd Electrical Test	100%	Functionality, Leakage
	Incoming Elec. Test	100%	Functionality, Leakage
	NV RAM Assembly		
	Electrical Test	100%	Functionality, Timing, All DC, Lithium Voltage

NV RAM ASSEMBLY EXPANDED FLOW
Figure 6



FLOW	PROCESS	FREQUENCY	PARAMETERS
	DS1218 & RAM Assembled Onto Circuit Board		
	Electrical Test	100%	Leakage
	Cell Attach		
	Epoxy Encapsulation		
	Visual Inspect	100%	Appearance

PERFORMANCE CHARACTERISTICS

The following section outlines several important performance characteristics of the DS1220 family. The data shown are samples from engineering testing performed during product development. These examples focus on perfromance characteristics determined by the controller chip and its interaction with the RAM and lithium cell.

As mentioned previously, one important function of the controller chip is to provide a switch to direct power from external V_{CC} or the lithium source, depending on whichever is greater. The typical I-V characteristics of the switch between external V_{CC} and the RAM is shown in Figure 7. Since this switch is implemented as a large MOS transistor, some voltage drop is unavoidable as a result of the transistor's channel resistance. Minimizing this drop important for optimum performance and reliability. This is done through proper transistor sizing, biasing voltages, and setting stringent test limits on the power requirements of the RAMs. A typical DS1220 draws an active current of 25-30 mA, resulting in a voltage drop across the switch of less than 0.2 volts.

POWER SWITCH I-V CHARACTERISTICS V_{CCI}-V_{CCO} VOLTAGE DROP Figure 7

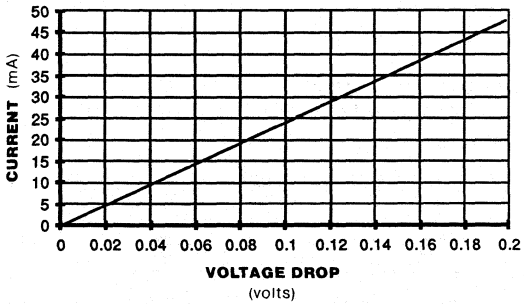
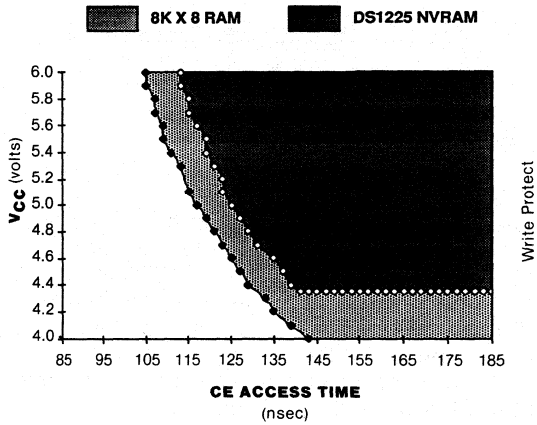


Figure 8 illustrates the typical AC performance characteristics of a DS1225-20 (200 ns). The influence of the DS1218 controller chip is clearly shown. During normal power supply conditions the NV RAM operates as a standard Bytewide SRAM. The Chip Enable command is passed through the controller to the RAM and the unit is powered by external V_{CC}. The CE propagation delay through the controller can be seen in Figure 8 as the difference in access time between the RAM (tested as a stand-alone unit) and the NV RAM (with the same RAM integrated into it).

Whenever the external V_{CC} supply falls below the write protection trip point voltage (V_{tp}), the controller will inhibit Chip Enable, thus forcing the RAM into standby and preventing all Read or Write operations. In Figure 8 this occurs at $V_{CC} = 4.3$ volts.

As Figure 8 shows, the total access time of the NV RAM during normal operation is the sum of the SRAM access time and the CE propagation delay through the controller. Figure 9, below, illustrates how the access time varies with temperature.

CHIP ENABLE ACCESS TIME VS. VOLTAGE $T_A = 25°C$ Figure 8



TYPICAL ACCESS TIME VS. TEMPERATURE $V_{CC} = 4.5V$, $V_{IH} = 2.2V$, $V_{IL} = 0.8V$ Figure 9

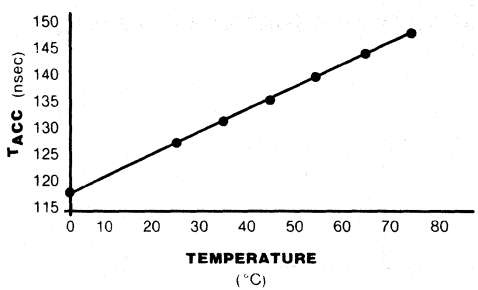
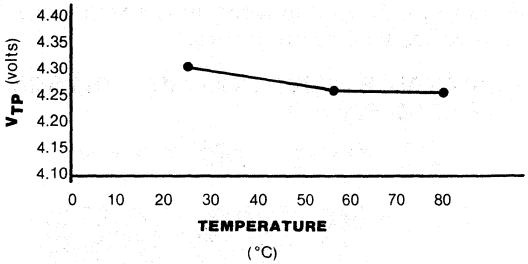


Figure 10 shows the write protection trip point voltage as a function of ambient temperature.

TYPICAL WRITE PROTECT VOLTAGE VS. TEMPERATURE Figure 10



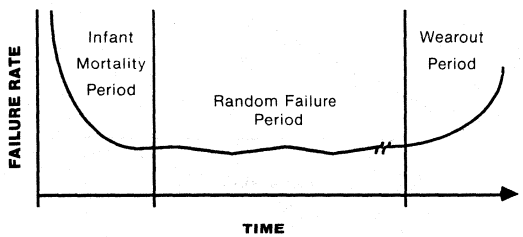
RELIABILITY DATA

OPERATING LIFE

The following section summarizes the estimates for the operating life failure rates and expected lifetimes of the DS1220 family. A distinction must be made between the mean time to failure and the predicted lifetime of these parts. To better understand the difference, a brief introduction of some basic reliability principles is helpful.

If the failure rate for an electronic component is calculated on a per-unit-time basis and plotted against a continuous time scale, the resulting chart will generally take the form of a "bathtub" curve, as shown in Figure 11.

RELIABILITY LIFE (BATHTUB) CURVE Figure 1



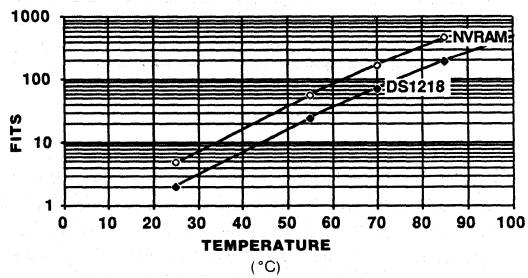
The curve is usually divided into three regions, each differing in frequency of failure and failure cause.

The first region is the infant mortality period. It is characterized by a high initial failure rate falling over time. These failures show up early in usage. They are usually associated with latent manufacturing defects and introduced during the process or assembly of the devices.

Dallas Semiconductor has incorporated high temperature, high voltage burn-in into the production flow. This acts as an effective screen, removing potentially defective units before they are shipped. This is performed on 100% of all units, thus eliminating the high failure rate during early life and removing the infant mortality period as a region of concern to the user.

After the infant mortality period, the failure rate reaches a low and nearly constant value. This is the random failure period which makes up the useful portion of the life of the circuit. Here the failures result from the limitations inherent in the design process.

NV RAM FAILURE RATE DURING OPERATING LIFETIME VS. AMBIENT TEMPERATURE Figure 12



Failure rate predictions for this region are usually obtained through accelerated reliability testing techniques. High voltage and/or temperature stresses are used to accelerate the failure mechanism so that a statistically significant number of failures are seen over a shorter period of time. Typical IC life studies are performed at 125°C for 1000 hours and the resulting failure rate is extrapolated to system use conditions through the Arrhenius mode. The Arrhenius model expresses the re-

lationship of failure rate to temperature as:

$$F1 = F2 * \text{Exp}[(Ea/k) * (1/T1 - 1/T2)]$$

Where:
F1 = Failure rate at T1 (expressed in °K)
F2 = Failure rate at T2 (expressed in °K)
Ea = Activation energy (electron volts)
k = Boltzmann's constant

Figure 12 illustrates the estimated failure rate for the DS1220 for the random failure period of its lifetime. These curves are based upon Arrhenius model extrapolations of life tests performed on the DS1218 controller circuits and the CMOS static RAMs used in the NV RAMs. Because of the temperature range limitations of the lithium cell, 125 °C operating life testing cannot be performed on complete NV RAMs.

The wearout period is characterized by a sharp rise in the failure rate over time as devices wear out physically and/or electrically. There is a very wide range in estimated lifetimes for various semiconductor and electronic components as well as a wide range in the failure mechanisms causing wearout. Some EEPROMs wear out after only a few thousand write cycles, caused by charge trapping in thin tunneling oxides. Other components may last for many years so that wearout isn't even a practical concern.

The wearout of the lithium cell representing the limiting item in the lifetimes of the DS1220 family of products. Two modes of wearout have been identified in lithium cells and should be considered independently, as each can limit the NV RAM lifetime depending upon the system application.

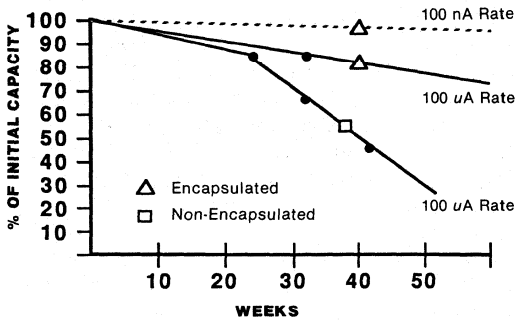
If the system is always powered-up and the lithium cell is used for memory retention for only short periods of time, the lifetime of the NV RAM will be limited by the shelf life of the battery. Extensive work has been performed studying the shelf life characteristics of the polycarbonmonofluoride lithium cell and two mechanisms have been identified which eventually contribute to end-of-life failures.

The first mechanism, which limits the cell's lifetime in many applications, involves the gradual diffusion of the electrolyte through the polypropylene seal. As this occurs the internal resistance of the cell increases since the separator is drying out and the number of charge carriers is becoming depleted. This mechanism is thermally activated; thus it is ongoing even when the battery is not being used. It results in a degradation of the cell's capability to deliver current at high rates and is significant for load requirements above 10 *u*A. The bottom curve in Figure 13 shows the impact of this mechanism for a sample of cells under storage at 85 °C. After various times in storage, sample cells were discharged at a 100 *u*A rate to determine their remaining capacity. The second curve shows the Impact of the epoxy encapsulation around the cell as in the DS1220 family of products. The epoxy acts as a second seal, helping to retard the diffusion of electrolyte. This slows the reduction of cell capacity by roughly a factor of four.

The lithium cell was designed to be lifetime-limited by the amount of lithium in the anode cap. Thus as lithium is consumed by current drain or other factors, the capacity is reduced until there is no lithium remaining. During this experiment analysis of the failing cells showed significant lithium remained. The apparent capacity loss was due to the increase in internal resistance. When a higher impedance level was applied to the failing cells, their output voltage was restored to a nominal level.

Thus, for current loads of 100 nA or less, as in the DS1220 family, this mechanism does not limit the lifetime of the battery. The expected reduction of capacity (for an encapsulated cell) at high temperature for 100 nA loads is shown in the top curve of Figure 13.

LITHIUM CELL CAPACITY VS. STORAGE TIME $T_{AMBIENT} = 85°C$ Figure 13



The second mechanism which can limit the lifetime of the cells is lithium consumption. This can take place with or without current drain being applied. If the system has been powered down (standby mode) so that data retention must be supported by the cell, lithium will be consumed at a rate proportional to the current load. The data retention lifetime in this mode can be calculated in the following manner:

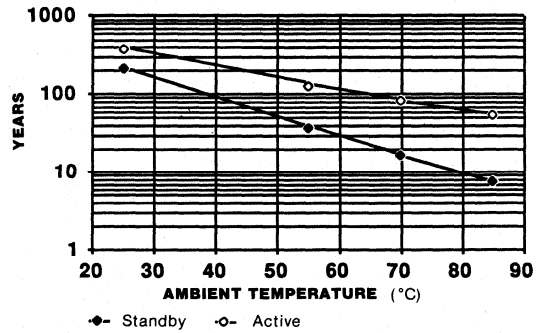
Assumptions:
Cell capacity = 35 mAhr
Temp = 25°C
RAM + Controller leakage current = 15 nA @5.75V

Calculated Lifetime
= (35E – 3/15E – 9) hours
= 2.33E + 6 hours
= 266 Years

The above calculations have been repeated for the DS1220 as a function of ambient temperature, and are plotted in Figure 14. The slope of the line is determined by the temperature characteristics of the leakage currents which have been found to increase by approximately 2.2 for every 10°C rise. This curve (labeled as "Standby") represents the expected lifetime of a DS1220 under constant data retention mode. If, on the other hand, the system is always powered up, the expected lifetime of the DS1220 is represented by the curve labeled as "Active." This curve is based upon experimental observations of lithium consumption as a function of shelf life under unloaded conditions.

These curves represent both extremes of system use conditions, one with the RAM always being powered by the lithium cell and the other never powered by the cell. It should be noted that the worst case condition, sustained high temperature with no V_{CC}, is a situation which almost never occurs in a practical application. The real use conditions should fall somewhere between these curves, depending upon the specific application. Laptop computers, for example, may require the RAM to remain powered by the lithium cell for prolonged periods of time, whereas a mainframe computer would require data retention only during short periods of power loss. To estimate the expected life for a specific application, a weighted average should be taken of the time in "Standby" mode and the ambient temperature.

EXPECTED LITHIUM CELL LIFETIME VS. TEMPERATURE Figure 14



ENVIRONMENTAL TESTING

The following section briefly outlines the results of various environmental tests performed on the DS1220. As a general rule, Mil. Std. 883B was used as the reference for establishing the specific test conditions. In some cases conditions have been altered due to specific limitations of the lithium cells. All read points included visual as well as full electrical testing (the only exception being the elimination of data retention testing for those units built without lithium cells).

TEMPERATURE CYCLING—DS1220

Test Conditions:
−55°C to +70°C, 15 min. each temp.

CYCLES	SAMPLES	FAILURES
10	100	0
50	100	0
100	100	0

THERMAL SHOCK—DS1220 W/O LITHIUM CELLS

Test Conditions:
0°C to +100°C, 5 min. each temp.
Transfer time 10 sec.

CYCLES	SAMPLES	FAILURES
30	28	0

HIGH TEMPERATURE, HIGH HUMIDITY

Test Conditions:
Ambient Temp. = 70°C
Relative Humidity = 95%

HOURS	SAMPLES	FAILURES
48	178	0
168	178	0
500	59	0

Dallas Semiconductor
Silicon Timed Circuit Detail

Technology

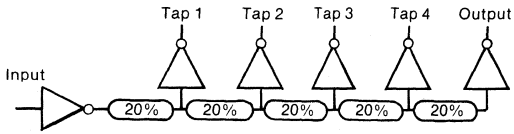
SILICON TIMED CIRCUIT DETAIL

PRODUCT DESCRIPTION

The DS1000 Series delay lines have five equally spaced taps providing delays from 20 ns to 500 ns. These devices are offered in standard 14-pin Dual In-Line Package (DIP). State-of-the-art laser technology is used to program timing parameters by directly writing nonvolatile bits into silicon. This all-silicon solution achieves higher reliability and lower cost than older hybrid techniques. The DS1000 Series delay lines provide an accuracy of ±5% or ±2 ns, whichever is greater, with a temperature coefficient of <1500 PPM/°C over the operating temperature range of 0°C to 70°C.

The delay line produces a TTL output level equivalent to the input after a fixed delay as specified by the part number. Each output has the capability of driving up to 10 74LS loads. Figure 1 illustrates the logic of the silicon delay line and Table 1 matches part number with delay time.

DS1000 LOGIC DIAGRAM Figure 1



PART NUMBER VS. DELAY TIMES Table 1

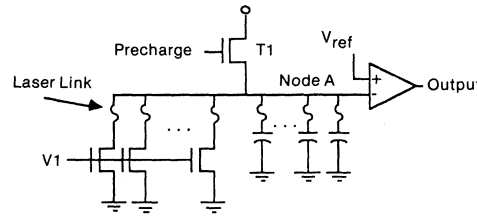
PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	OUTPUT
DS1000-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1000-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1000-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1000-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1000-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1000-250	50 ns	100 ns	150 ns	200 ns	250 ns
DS1000-500	100 ns	200 ns	300 ns	400 ns	500 ns

The basic technology used to produce the DS1000 Series delay line is similar to laser redundancy, which has been used extensively for high density MOS memories. The inherent reliability of using lasers to cut polysilicon links has thus been proven in the millions of memory components shipped using this technology.

Figure 2 illustrates the fundamental delay unit used in the DS1000 Series. Node A is precharged high by transistor T1. V1 is later switched high in response to the input. The V1 high level is set by an internal reference voltage which is temperature compensated to provide a minimum temperature coefficient. Node A is then discharged to ground at a rate determined by the value of V1 (high) and the number of pull-down transistors and load capacitors connected to it. An Op-Amp is used as a comparator and output driver circuit to provide an output waveform independent of the delay.

Each delay is programmed to the desired value by selectively disconnecting either pull-down transisitors or load capacitors from Node A. This is done with a short pulse Neodymium:YAG laser-cutting minimum-width polysilicon fuses.

BASIC DELAY CIRCUIT Figure 2



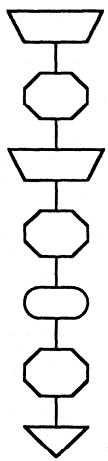
PROCESS FLOW DESCRIPTION

Figure 3 below describes the basic process flow for the DS1000 Series. Laser programming of each circuit is done in wafer form at probe test. This test utilizes a hardware setup consisting of a positioning laser/wafer prober and a functional/timing tester. The hardware operates in an interactive mode between the tester and the laser, first measuring the initial delays, programming with the laser, and retesting to guarantee conformance to the specifications.

After assembly, each unit is retested, checking all DC parameters, before undergoing a high temperature (125 °C) burn-in. This is effective in improving device reliability by screening infant mortality failures and insuring timing stability.

After burn-in each unit is retested to guarantee conformance to all DC, functionality and timing specifications.

DS1000 PROCESS FLOW Figure 3



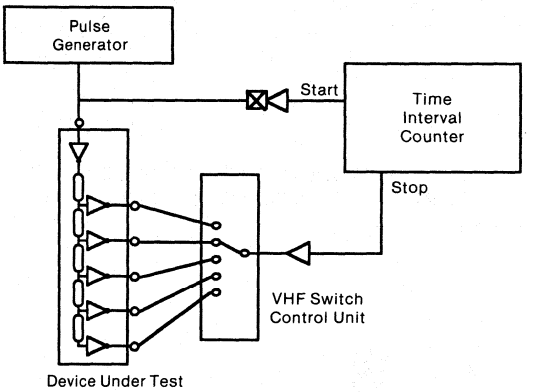
FLOW	PROCESS	FREQUENCY	PARAMETERS
	Wafer Fabrication		
	Interactive Wafer Probe & Laser Write	100%	All DC Tests, Rising & Falling Time Delays
	Assembly & Brand		
	1st Electrical Test	100%	I_{CC}, Input Leak. Output Current
	Burn-in	100%	12 Hrs., 7 volts, 125 °C
	2nd Electrical Test	100%	All DC Tests, Rising & Falling Time Delays
	Customer		

TEST SET-UP DESCRIPTION

Figure 4 illustrates the hardware configuration used during laser programming for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each output. Each tap is selected and connected to the counter by a VHF switch control unit.

The measurement set-up is calibrated by time domain reflectometry techniques. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TIME DELAY MEASUREMENT SET-UP
Figure 4



PERFORMANCE CHARACTERISTICS

Samples of DS1000-100 devices were characterized over the temperature range from −20 °C to +90 °C. The units were run at V_{CC} = 5.0V using a 1 *u*sec square wave input. The typical performance characteristics for each output as a function of temperature has been normalized and graphed in Figure 5 below.

TEMPERATURE PERFORMANCE OF DS1000
NORMALIZED DELAY VS. TEMP.
Figure 5

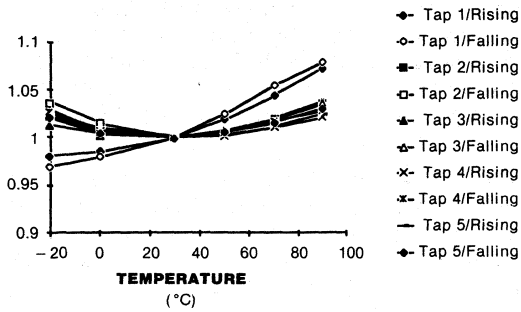
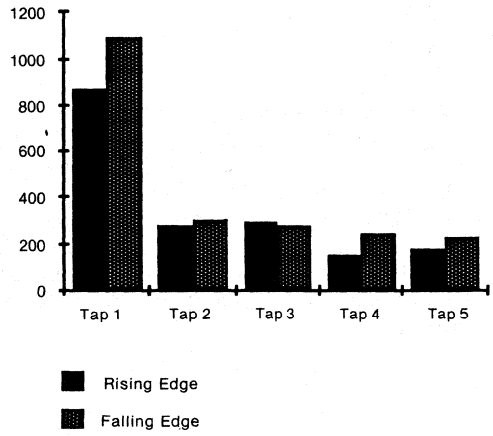


Figure 6 illustrates the typical temperature coefficients for each delay output. This number is calculated by taking the difference between the maximum and minimum values for the delay over the 0°C to 70°C range and dividing by the product of 70 (the change in temp.) and the value of the delay at 30°C.

TC = (Max − Min) / (70 * Delay @ 30°C)

DS1000 TEMPERATURE COEFFICIENTS
TYPICAL TEMP. COEFF. (0°C to 70°C)
PPM/°C Figure 6



ESD TESTING RESULTS

Table 2 summarizes the electrostatic discharge test results for DS1000. All data was taken on an IMCS Model 2400 ESD Simulator according to Mil. Std. 883C Method 3015 (1.5 KΩ, 100 pF). Each pin was tested with both positive and negative polarity referenced to ground. Other pins (except for ground) are left floating during test. Testing begins at +500 volts, then alternates to −500 volts, each time with 5 zaps per pin. The test voltage is increased by 500 volts until 2000 volts or a failure is seen.

A pass/fail determination is made by testing for functionality, leakage to V_{CC} or GND, or a change in I_{CC} or output drive currents.

ESD TESTING RESULTS Table 2

PART #	INPUT	TAP 1	TAP 2	TAP 3	TAP 4	OUTPUT
1	2000V	2000V	2000V	2000V	2000V	2000V
2	-2000V	—	—	—	—	—
3	-2000V	—	—	—	—	—
4	-2000V	—	—	—	—	—
5	2000V	2000V	2000V	2000V	2000V	2000V
6	2000V	2000V	2000V	2000V	2000V	2000V
7	2000V	2000V	2000V	2000V	2000V	2000V
8	2000V	2000V	2000V	2000V	2000V	2000V

Parts #2, 3 and 4 failed functionality after 5 zaps on the input pin at −2000 volts; thus, valid data could not be collected on the output pins of these devices. No other ESD failures were observed from the sample.

All units tested exceeded the minimum requirements for Mil. Std. 883C condition B. Condition B devices are acceptable for general use in military equipment.

PERFORMANCE STABILITY TEST RESULTS

Table 3 lists the measured delay times for a sample group of DS1000 devices. Measurements were made just after laser programming, and before and after a 12-hour, high-temperature burn-in to evaluate the stability of the delay circuits during high-stress conditions. *The average change in delay across burn-in was less than 0.3%.* The final error from target value was less than 2.5%.

MEASURED DELAY TIMES BEFORE AND AFTER BURN-IN Table 3

TAP	EDGE	POST LASER	PRE-BURN	POST-BURN	% CHANGE	FINAL ERROR
1	Rising	20.055	20.195	20.151	0.22%	0.76%
	Falling	19.956	20.211	20.178	0.16%	0.89%
2	Rising	40.594	40.249	40.113	0.34%	0.28%
	Falling	40.443	40.334	40.220	0.28%	0.55%
3	Rising	61.093	61.057	60.856	0.33%	1.43%
	Falling	60.613	60.255	60.120	0.22%	0.20%
4	Rising	81.708	91.987	81.729	0.31%	2.16%
	Falling	80.080	79.124	78.963	0.20%	1.30%
5	Rising	102.046	102.690	102.411	0.27%	2.41%
	Falling	99.869	99.544	99.271	0.27%	0.73%

HIGH TEMPERATURE OPERATIONAL LIFE

Life testing was performed on a production sample of DS1000 units according to the following conditions:

Stress Conditions:
Temp = 125 °C
V_{CC} = 7 Volts
Cycle Time = 1 *u*sec
Input Levels = 0V/3V

Units = 200

READ POINT	TEST YIELD	FAILURE MECHANISM
48 Hrs	199/200	Input Leakage—ESD Damage
168 Hrs	199/199	
500 Hrs	199/199	
1000 Hrs	197/199	Open Outputs—both units

This corresponds to a long-term life failure rate of 0.007%/K hours at an operating temperature of 55°C.

Dallas Semiconductor
Nonvolatile Static RAM

Application Note-1

NONVOLATILE STATIC RAM

Vast resources have been expended by the semiconductor industry trying to build a nonvolatile Random Access Read/Write Memory. The effort has been undertaken because nonvolatile RAM offers several advantages over other memory devices—DRAM, Static RAM, Shadow RAM, E^2PROM, EPROM and ROM—which were developed to meet specific applications needs.

Characteristics of the ideal nonvolatile RAM are: low power consumption; higher performance; greater reliability; higher density; and the ability to be used in any semiconductor memory application.

While the various memory components designed to date are not appropriate for the ideal memory scenario, each excels in meeting one or more of the sought after attributes (Figure 1).

Figure 1 **MEMORY ATTRIBUTES**

	COST	INTERFACE EASE	NON-VOLATILE	DENSITY	PERFOR-MANCE	READ/ WRITE	DATA RE-TENTION
DRAM	+ +			+ +	+	+ +	
STATIC RAM	+	+ + +		+	+ + +	+ + +	
SHADOW RAM			+		+	+	+
E^2PROM			+				+
EPROM	+ +	+ + +	+ +	+ +			+ +
ROM	+ + +	+ + +	+ + +	+ + +	+		+ + +

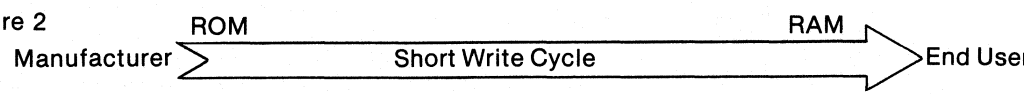
+ = Degree of Excellence

Many types of memories have been devised to meet varying application needs. Nonvolatile Read/Write Random Access Memories can be substituted for all memory types independent of applications.

For example, NMOS DRAM memory provides performance and density, but, on the down side, must be constantly refreshed to retain data. At the opposite extreme are ROMs, offering nonvolatility and density, but lacking the ability to be updated with new data because information is burned in only once. Between these two are a wide range of devices that fulfill some characteristics of the ideal memory.

Two popular devices, E^2PROMs and Shadow RAMs, are designed to emulate a static RAM but also have the ability to retain data after a power loss. But despite their capability to retain data, both E^2PROMs and Shadow RAMs fall short of meeting the industry's needs for several reasons (Figure 2).

Figure 2



Long Write Cycles prevent E^2PROMs from emulating RAM, making them less than ideal memories.

Most notably, the E^2PROM requires a special write cycle. The E^2PROM's inability to support standard write cycle hinders performance in applications where memory is updated immediately as new data is available.

Another problem with E^2PROMs is their wear out mechanisms. These raise reliability concerns due to the limited number of write cycles allowed—sometimes as few as 10,000. If a static RAM with a 200 ns cycle time had this limitation, it would wear out in a mere 20 ms. An application that requires constant updating, such as the buffer memory of a cashier's checkout terminal or a printer, the E^2PROM's wear out mechanism is not acceptable.

Shadow RAMs, on the other hand, have been developed to overcome long write cycles and avoid wear out, but still require special store and recall operations and to date are at densities of less than 4K bits. In addition, the majority of available Shadow RAM devices do not provide a write protection mechanism to prevent losing data when the system experiences out-of-tolerance conditions due to a power loss.

Finally, because of the complexity of programming circuits, the cell structure and the special process technology required, the density of both E^2PROMs and Shadow RAM have not kept up with industry demands.

In systems requiring store-and-forward data, the nonvolatile RAM must provide the desired fast write cycle as well as protection of memory in the event of a power loss. Despite the promise of such a memory device and the effort invested by the industry, the ideal nonvolatile RAM is just now becoming available.

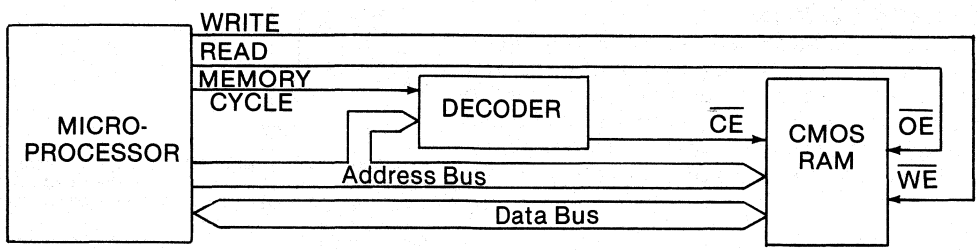
To provide the ideal nonvolatile RAM, Dallas Semiconductor has combined two technologies—intelligent CMOS control circuitry and lithium energy—to offer the first available high-density nonvolatile memory.

Two devices, the DS1220 (2K × 8 bits) and the DS1225 (8K × 8 bits), use this combination and a CMOS static RAM to provide a nonvolatile Random Access Memory solution at a density of 64K bits. These memory devices are the most appropriate answer to date because of the beneficial qualities of CMOS static RAM.

CMOS static RAMs currently available have read and write cycle times of 100 ns, which exceed most system requirements. This alleviates the problem of the E^2PROM, because there are no wear-out mechanism or write cycle limitations.

Static RAMs are also the easiest to use and interface because the pin-out configurations are standard throughout the industry. In fact, X8 or bytewide static RAMs can be interfaced directly to microprocessors (Figure 3). In addition, CMOS static RAMs offer low power in both active and standby modes, a characteristic sought by many designers. In most designs, RAMs remain in standby much of the time, keeping power consumption negligible. In the standby mode, current drain consists only of leakage currents in the tens of nanoamperes. The density of static RAM is presently at an impressive 8K × 8 or 64K bits and is doubling every two years.

Figure 3



Bytewide memories provide easy interface to microprocessors because of the X8 organization and control signal definition.

PUTTING LITHIUM AND RAM TOGETHER

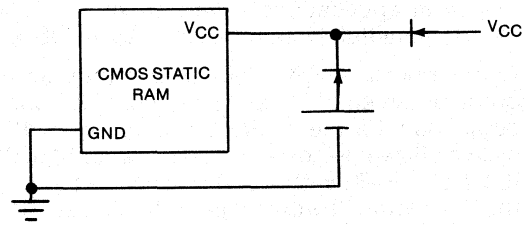
The minute leakage current of CMOS RAMs can be sustained with a backup energy source to yield a most attractive nonvolatile memory. However, the actual solution to the ideal nonvolatile memory involves more than just a CMOS memory and back up energy source (see Figure 4).

Battery Backup design schemes are many and varied. The increase in density and availability of low powered CMOS memories in recent years has made this approach even more attractive. Yet problems still exist with battery backup design due to battery packaging and a lack of the appropriate standard components to implement the support circuitry. One problem is providing isolation between the battery and power supply (see Figure 5). Diodes can provide isolation but produce a voltage drop which requires nonstandard power supplies and also subtracts from the battery voltage. A second problem is the circuitry required to detect power failure and write protect the memory. This additional circuitry must be powered from the battery. Unless these devices draw an extremely modest amount of current, battery selection changes drastically. In fact a current drain of even a couple of microamperes dictates the use of either rechargeable batteries or a replaceable battery scheme. If rechargeable batteries are selected, the recharging circuit can be costly and complex and the best rechargeable battery cannot compare with the electrochemical stability of the lithium primary cell. Even worse, replaceable batteries add maintenance and cost to an in-service system. Battery packaging has also been a serious limitation taking up valuable space and requiring special handling considerations to prevent discharge.

ENERGY SOURCE

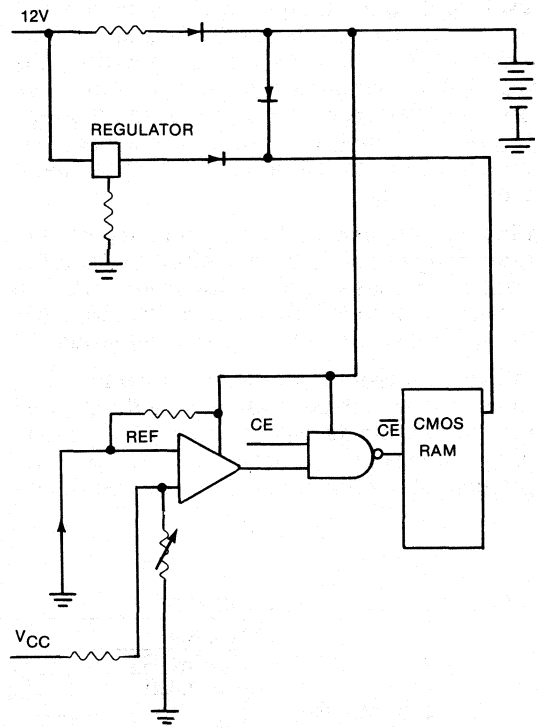
The energy source used to retain data in the ideal memory must be capable of outlasting the usefulness of the end product. The products use the extremely stable electrochemical system lithium polycarbon monofluoride with over 35 mA hours of energy reserve and

BATTERY BACKUP CIRCUIT? Figure 4



CMOS static RAM requires more than just a backup power supply. Data must also be protected during power transients to avoid garbled data.

Figure 5



Support circuitry required to produce power fail detection and write protection forces the need for a multicell rechargeable battery or a replacement lithium battery.

guaranteed shelf life greater than 10 years. The total energy cell load current used by the DS1220 and DS1225 is less than 100 nA at 25 degrees C. This gives a calculated lifetime of more than 40 years in the absence of externally applied power.

LITHIUM BATTERY BACK UP IS MORE RELIABLE

The lithium energy cell has raised concern about reliability and has been the object of much study[1]. Data taken on the energy cell used in the DS1220 and DS1225 indicates a failure rate less than 0.5% per three million device hours at 70 degrees C.

Additional life studies taken on the same lithium energy source encapsulated in the manufacture of the DS1220 and DS1225 have produced no failures in over 12 million device hours at 70 degrees C. The lithium energy cell, then, is ideal for commercial and industrial semiconductor applications.

RETROFITTING EXISTING DESIGNS

The pinout of the DS1220 and DS1225 is an established industry standard (Figure 6). The Joint Electronic Devices Engineering Council's Bytewide Version B Standard defines and upgrades from 2K × 8 in density to 32K × 8.

This standard accommodates RAM, ROM, UV EPROMs, and E^2PROMs. Because of the flexibility and upgradeability of bytewide memories, the number of existing sockets is in the hundreds of millions. Therefore, many system designs can accommodate direct replacement of RAMs, EPROMs, ROMs, and E^2PROMs with the DS1220 and DS1225. These new solutions add real time programmability and/or density upgrades to existing system without redesign. Real time programmability gives the system the ability to be personalized by the end user. In other words, the nonvolatile RAMs can be retrofitted into existing design without change to existing hardware. This retrofitting offers a cost-effective, practical solution for companies who have invested in other memory devices that are less than ideal for their needs. For example, a design using conventional static RAM can be upgraded to nonvolatile memory by substituting a DS1220 or DS1225 for the RAM memory.

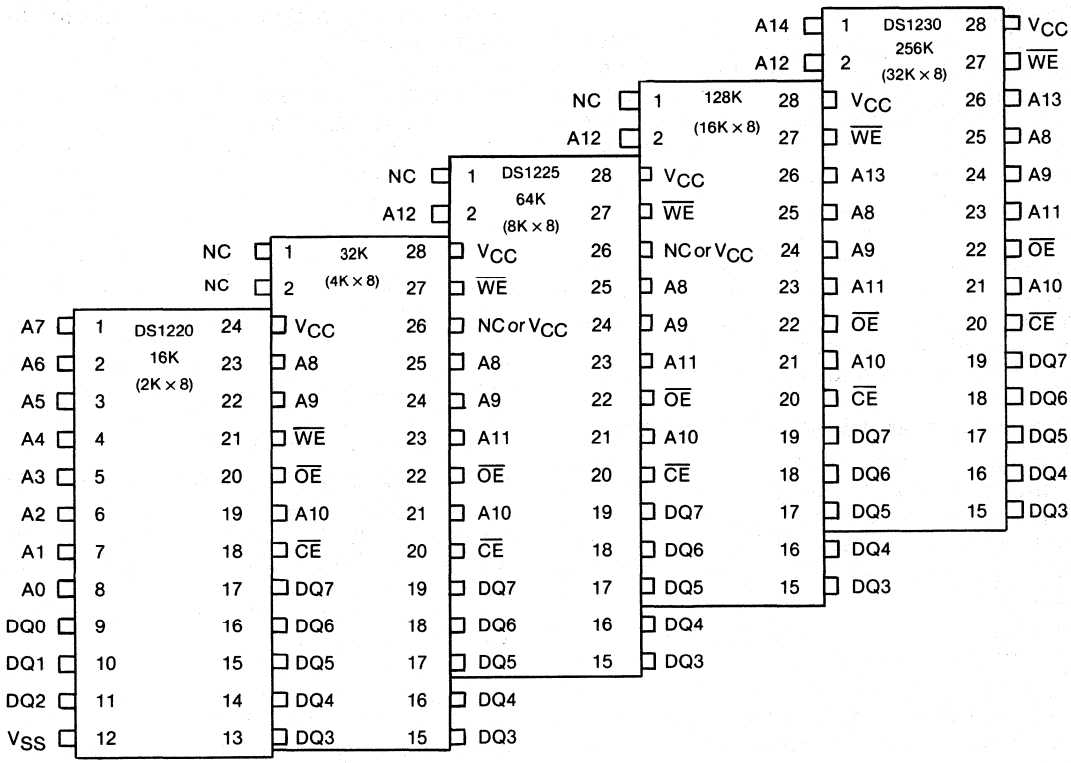
IN-CIRCUIT PROGRAMMABILITY

The advantages of nonvolatile RAM can be related to the capability of software. Modern systems seek customization for the cost of standard product. In this aspect, software can be adapted in this system to perform specialized functions. It is even possible to totally modify a system personality over the telephone. In-circuit programming also reduces maintenance cost by eliminating service calls to update software. Software stored in RAM can be updated as often as necessary, depending on the configuration or application of the system.

In the immediate future, the density of a nonvolatile CMOS static RAM will continue to increase. By 1986, a 32K × 8 version of the nonvolatile RAM will be available from Dallas Semiconductor. In addition, Dallas Semiconductor will offer a watch function and security options in combination with nonvolatile RAM. Still other devices will be introduced using special packaging techniques to add portability to nonvolatile memories. These packages will offer designers and end users the ability to give their systems unique solution characteristics for value added configurations.

[1]Louis J. Hart and Theodore Ciobanu, "Lithium Batteries for Memory Backup—An Evaluation Program at IBM," published in *Batteries Today*, Summer 1984 issue.

Figure 6 **Bytewide JEDEC Pinout**



Provides for density upgrade to 32K × 8

Dallas Semiconductor
User Insertable RAM

Application Note-2

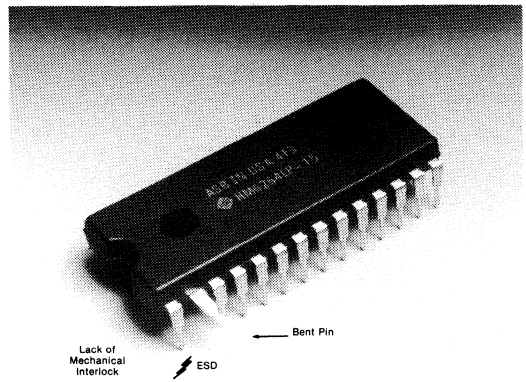
USER INSERTABLE NONVOLATILE RAM

Semiconductor packaging has precluded the handling of memory by the end users (Figure 1). There are many examples of equipment manufacturers ranging from consumer video game cartridges to speech recognition for industrial automation who have repackaged semiconductor memory to permit handling by the end customer. The underlying reason is to increase the flexibility of a mass produced piece of equipment. Game manufacturers found out that by producing one standard size video console they could meet the diverse interests of their customers with cartridges sold in the after market. More often than not the value of a piece of equipment is tied to how closely it can be adapted to serve a specific need (Figure 2). This is in conflict with the economics of mass production. When a design has no options, it would tend to be lower in cost but offer marginal application fit. Unlike mechanical, electronic equipment has an inherent advantage in adapting to diverse needs largely as a result of the microprocessor and its associated memory. In particular, the cost of creating uniqueness has been drastically lower with the availability of nonvolatile RAM. When nonvolatile RAM is packaged in a user-insertable format, even more possibilities are opened up (Figure 3).

Dallas Semiconductor produces user insertable nonvolatile RAM as an off-the-shelf component ranging from a 1000 bit DS1201 Electronic Tag to a 1 million bit cartridge (Table 1). Careful attention has been given during the design of these products to make them connect directly to microprocessor systems (Figure 4). Being solid state, these devices are rugged and suitable for harsh environments.

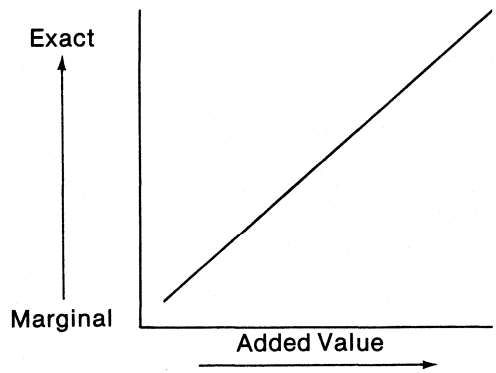
USER INSERTION PROBLEMS WITH CONVENTIONAL INTEGRATED CIRCUITS

Figure 1



APPLICATION FIT

Figure 2



BENEFIT OF NONVOLATILE RAM

Figure 3

- Procedure learning
- Adaptive control
- Automatic firmware updates
- Real time data capture

ADDED BENEFITS OF USER INSERTABLE MEMORY

- Improved application fit
- Eliminate costly service
- Simplified optioning
- Permits system to evolve
- After market sales

USER INSERTABLE MEMORY Table 1
TAGS

Part Number	**DS1201**	**DS1205**
Density (Bits)	1024	4096
Interface	Serial	Serial
Data Retention	10 Years	10 Years
Availability	Now	Future
Connection	5 Pin SIP	5 Pin SIP

CARTRIDGES

Part Number	**DS1217/ 16K**	**DS1217/ 64K**	**DS1217/ 128K**	**DS1217/ 196K**
Density (Bits)	16K	64K	128K	196K
Interface	Bytewide	Bytewide	Bytewide	Bytewide
Data Retention	10 Years	10 Years	10 Years	10 Years
Availability	Now	Now	Now	Now
Connection	30 Pos. Card Edge	30 Pos. Card Edge	30 Pos. Card Edge	30 Pos. Card Edge

Part Number	**DS1217/ 256K**	**DS1217/ ½M**	**DS1217/ 1M**	**DS1217/ 4M**
Density (Bits)	256K	512K	1M	4M
Interface	Bytewide	Bytewide	Bytewide	Bytewide
Data Retention	10 Years	10 Years	10 Years	10 Years
Availability	Now	Now	Now	Future
Connection	30 Pos. Card Edge	30 Pos. Card Edge	30 Pos. Card Edge	30 Pos. Card Edge

THE NONVOLATILE READ/WRITE CARTRIDGE

The DS1217 nonvolatile cartridge is a compact, rugged, and portable memory presently available in densities of 2K × 8, 8K × 8, 16K × 8, 24K × 8, 32K × 8 64K*x*8, and 128K × 8 (Figure 5).

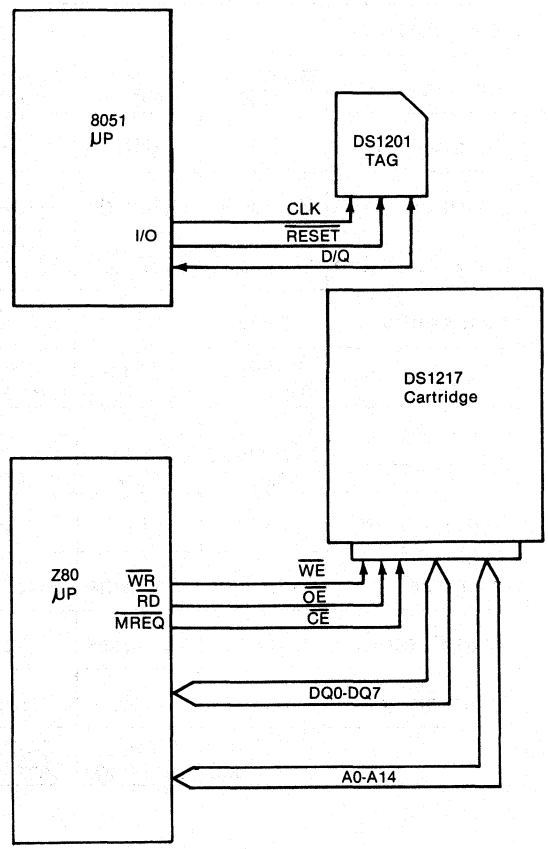
Density is expected to increase to 4M bit, 512K × 8 before 1987. All of the future high density cartridges will have the same package dimensions and connector pinout so that upgrades can be easily accomplished. Data is accessed randomly, one byte at a time via a 15 bit address bus and an 8 bit data bus. Data can be written or read from the cartridge in the same manner as regular static RAM with a read/write cycle time of 250 ns. Because the cartridge is nonvolatile, data is retained when the cartridge is removed from a system. Data retention is handled transparently inside the cartridge via an intelligent controller chip which safeguards data and directs an internal lithium energy source to memories when power is lost. Data is protected from inadvertent loss by preventing memory cycles when the external supply voltage is less than 4.5 volts. Data retention is accomplished by selecting the greater of two voltages, i.e., either the external supply (V_{CC}) or the internal lithium energy source. A switch is also provided on the cartridge which unconditionally protects data. When the write protection switch is turned on, the cartridge becomes read only and all write cycles to RAM are ignored.

The lithium energy source used is the extremely stable electrochemical system lithium polycarbon monofluoride. This energy system has the capacity and shelf life needed to retain data for well over ten years in the absence of external power. The lithium energy source has raised concern about reliability and has been the subject of much study[1]. Data taken on the energy source used in the DS1217 indicates a failure rate less than 0.5% per three million device hours at 25°C.

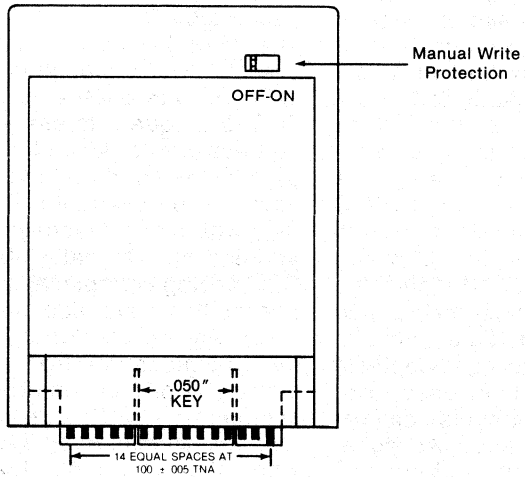
The edge connector on the cartridge has been arranged to meet the JEDEC Standard Bytewide 28-Pin Dip Socket, making it compatible with existing designs. The cartridge can be plugged into a 28-pin socket via a ribbon cable with a 30-position edge connector on one end and a 28-pin plug on the other (Figure 6). This ribbon cable can be purchased directly from AMP or from Dallas Semiconductor (DS9000). The AMP Part Number is 494940-1. The ribbon cable can be used to retrofit existing systems which use the bytewide socket adding nonvolatility, portability, and density upgrade.

DIRECT CONNECTION

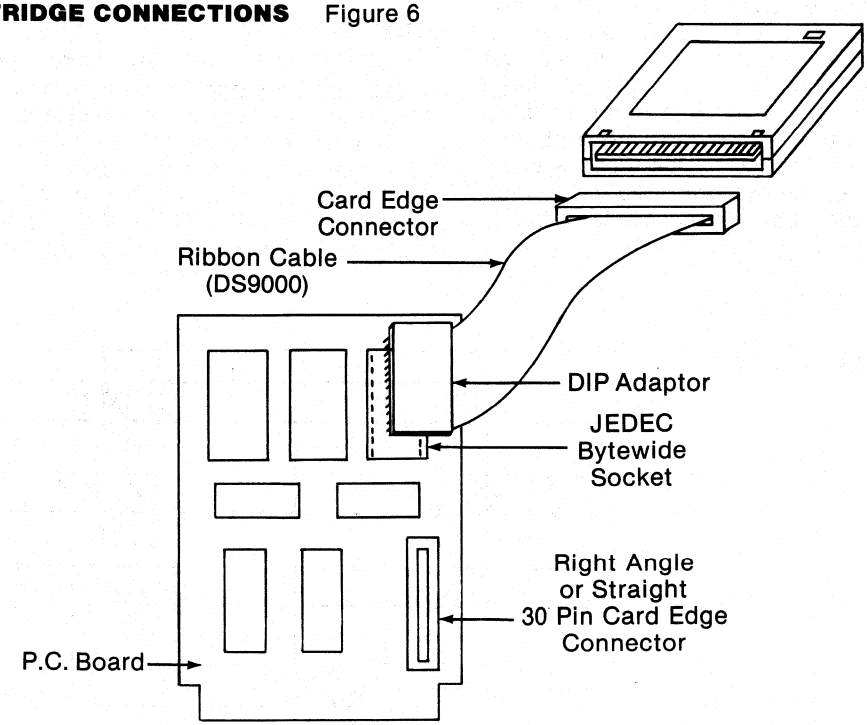
Figure 4



NONVOLATILE READ/WRITE CARTRIDGE — DS1217 Figure 5



CARTRIDGE CONNECTIONS Figure 6



Every precaution has been taken with the design of the cartridge to protect data integrity while handling. The case is made of durable impact resistant plastic capable of sustaining a three foot drop test on a concrete surface. The casing is designed to protect the internal electronics from dust, shock, and other elements of an adverse environment. The cartridge will operate over a wide temperature range of 0°C to +70° C and permit storage with data retention from −40° C to +70° C. Relative humidity can vary between 0 and 95% provided there is no condensation. The mating connector is plated with 50 u inches of gold over 150 u inches of nickel. When the proper mating receptacle (AMP Part Number 494940-1) is used, over 3000 insertions and withdraw cycles can occur without electrical degradation. All signal lines are recessed and the ground connection is extended on the mating connector to prevent electrostatic damage to internal components. The recessed signal paths and extended ground have the added advantage of enhancing data integrity when the cartridge is inserted and withdrawn while power is applied because the possibility of charge injection into the memory is eliminated. To further prevent garbled data while "hot plugging" the cartridge, two offset keys are provided. When both keys are used in the mating receptacle, data integrity is virtually assured.

OPERATION

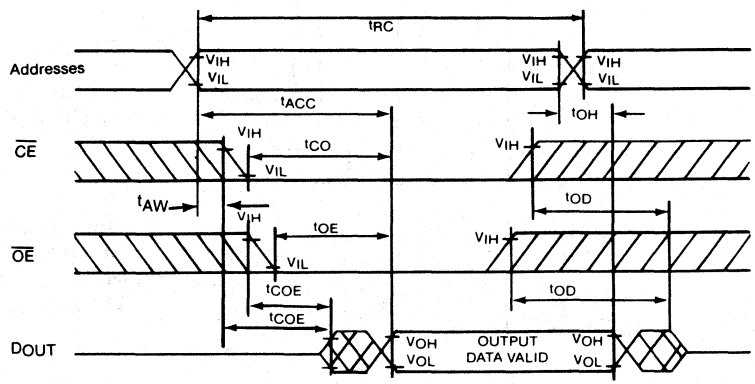
READ MODE

The DS1217 is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low) (Figure 7). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight date I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satified. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than or equal to 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

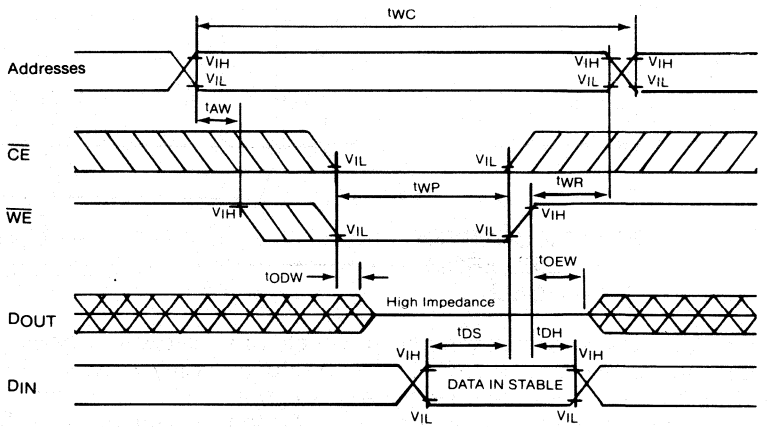
The DS1217 is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable (Figure 8). The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the

READ CYCLE Figure 7



write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{OWD} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

WRITE CYCLE Figure 8



DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts (Figure 9). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217 constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

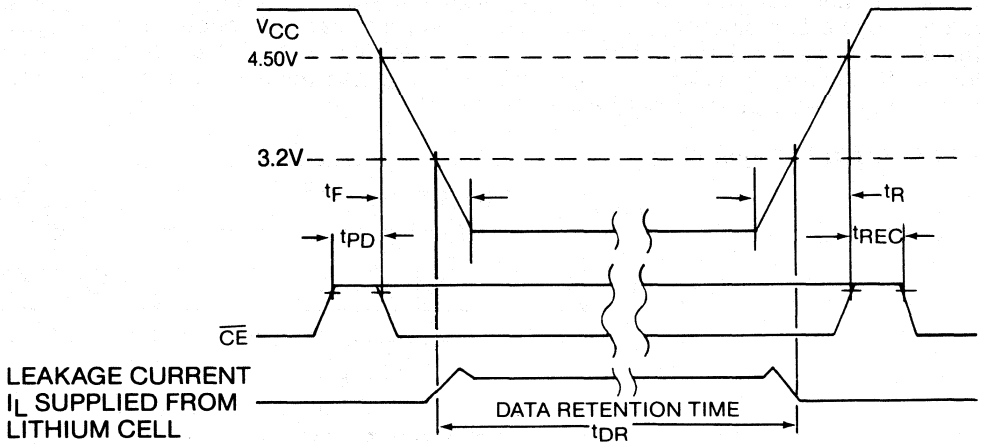
The DS1217 checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217 provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

OPTIONAL SECURITY FEATURE

Cartridges can be used to add features to a system and as such are often sold as value added extras. In these applications protection of software and guarding sensitive data is often important in avoiding competition. To date the problem of maintaining after market sales has been solved by special

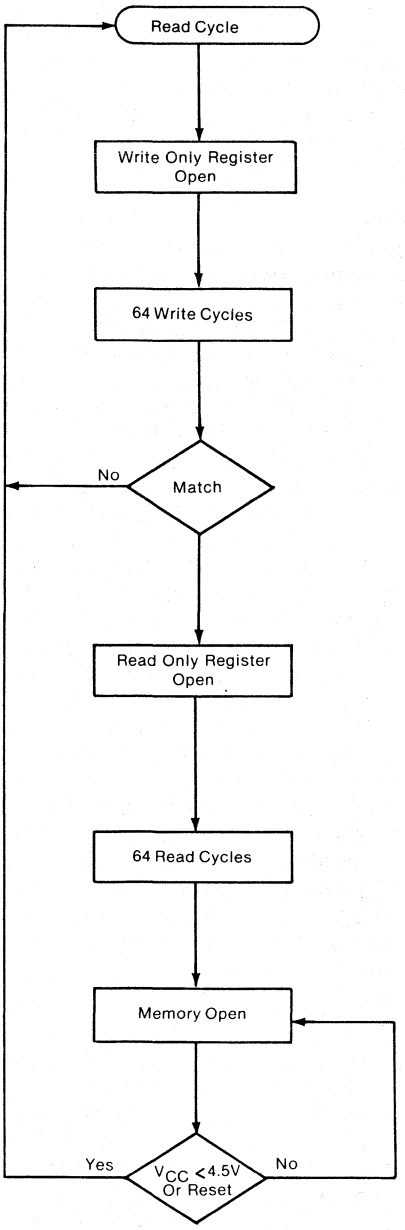
POWER-DOWN/POWER-UP CONDITION Figure 9



molded cases and connectors which are unique to each equipment manufacturer. These barriers are relatively easy to overcome by competitors. In contrast, Dallas Semiconductor provides standardized cases and connectors but employs laser technology to make silicon unique. This presents a far more formidable barrier to potential after market competitors and also reduces cost. Dallas Semiconductor cartridges have added security circuitry which makes it usable for only one manufacturer's specific application while maintaining the same form factor and connector system. When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the cartridge (Figure 10). A 64 bit access code must be consecutively written to the cartridge. Actual RAM locations are not written as the security option is intercepting the data rate until access is granted. Following the 64 write cycles a comparison is made to a 64 bit pattern uniquely defined by the user and programmed into the DS1217 by Dallas Semiconductor at the time of manufacture. This pattern can only be interrogated by an intelligent controller within the cartridge and cannot be read by the user. When a correct match is found, the next part of the security sequence begins by reading a 64 bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1217 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user defined read only register is available. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register may be used by software to determine if the cartridge will be permitted to be used with that particular system. After the 64 read cycles the cartridge is unlocked and all subsequent memory cycles will become actual memory accesses based on address inputs. This procedure prevents second party encroachment.

The security feature can also be used for bank switching in and out multiple cartridge in the same memory address space. Entrance to the desired cartridge would take place exactly as described above. Since each cartridge can have a different security code, only the one with the exact pattern match would allow access. To change from one cartridge to another, the reset line must be driven low long enough to exit from the active cartridge. A different cartridge could then be entered by matching the security code.

SECURITY SEQUENCE Figure 10



THE ELECTRONIC TAG

The DS1201 is a miniature nonvolatile read/write memory system. The Tag is organized as a 128 x 8 memory. However, data is accessed in a serial manner to reduce pin count, and to simplify interface requirements while enhancing the reliability of connection. In fact, the Tag can be carried in your pocket, dropped in the water, and even stepped on, and still retain data. Low pin count combined with a special mechanical form factor has been used to make the device compact, rugged, and user insertable.

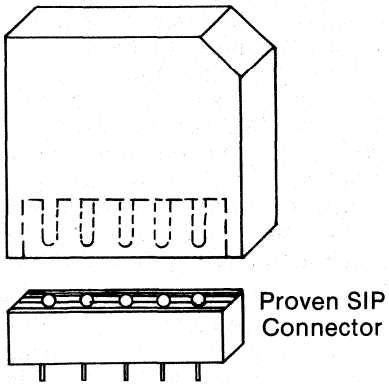
The Tag is permanently powered by a lithium polycarbon monofluoride energy cell which retains data in the absence of power. This energy cell is the same type as that used in the cartridge differing only in size and energy capacity. When connected in a system, power can be supplied via the reset signal or the V_{CC} pin. Reset current of only 2 mA supplies all the energy needed by the Tag. Reset is also used to initialize and terminate all communications with the Tag.

The Tag is designed to be plugged into a standard 5 pin 0.1 inch center SIP receptacle (Figure 11). A key is provided to prevent the Tag from being plugged in backward (Figure 12). Contact to the Tag can be determined to insure connection integrity before data transfer begins. Clock, $\overline{\text{RESET}}$, and data INPUT/OUTPUT all have 25K Ohm pull down resistor to ground which can be sensed by a reading device. While the Tag is designed to be a user insertable device it is not limited to those applications. The Tag can be used inside a system using the same 5 pin SIP strip and become a permanent 1K nonvolatile memory.

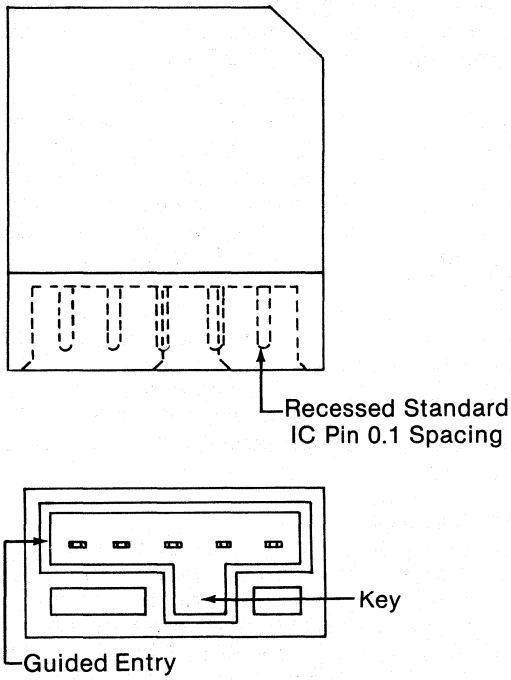
OPERATION

The block diagram (Figure 13) of the Electronic Tag illustrates the main elements of the device: namely, shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the shift register providing both address and command information. Each bit is serial input on the rising

TAG CONNECTIONS Figure 11



TAG Figure 12



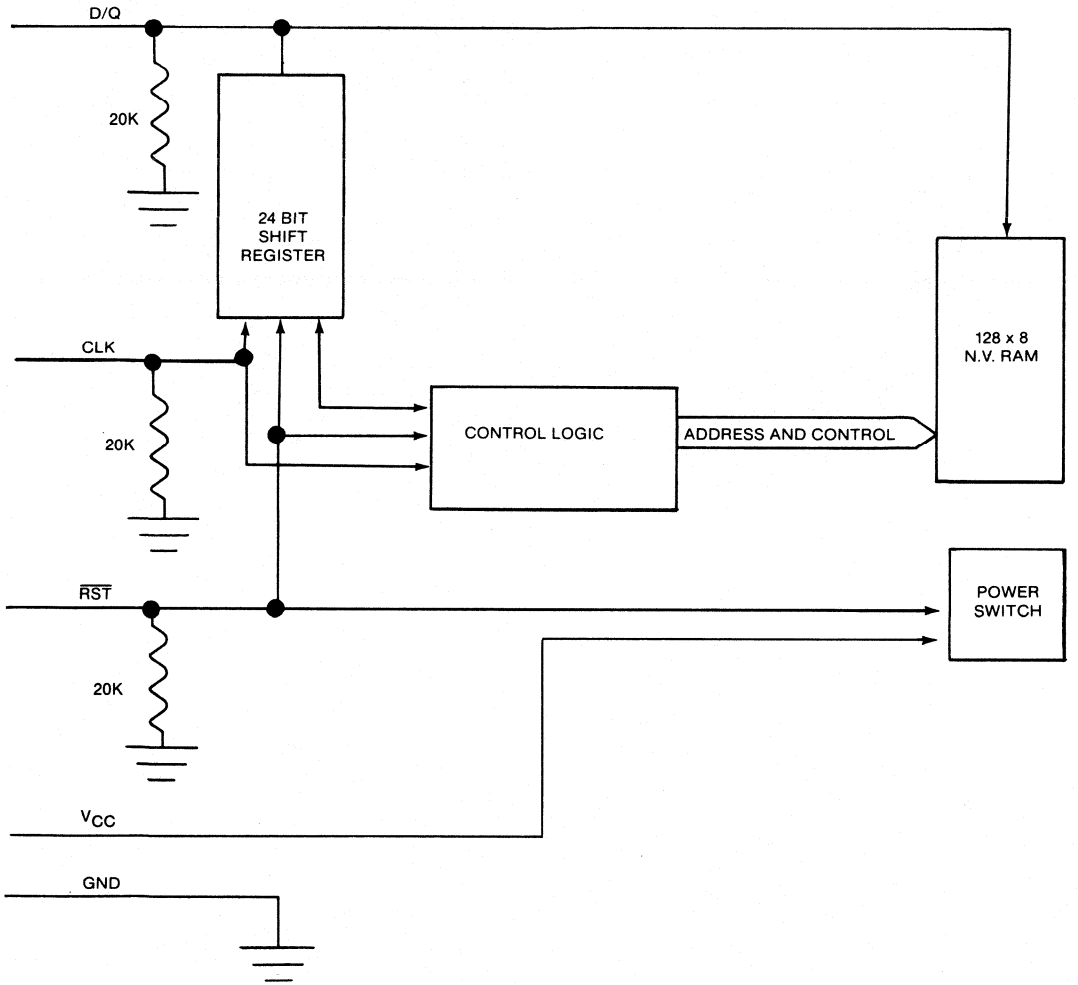
edge of the CLOCK input. Seven address bits specify one of 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKS which load the shift register additional CLOCKS will output data for a read, or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

APPLICATIONS

The portable computer is an example of many applications which can take advantage of user insertable nonvolatile memory. The portable computer approaches the power and capability of a desk top personal computer with the notable exception of mass data storage. The most popular type of mass data storage is the floppy disk. Floppy disks are dense and miniature, but suffer from two drawbacks. First, floppy disks are fragile, making their use prohibitive in many applications. Second, the mechanism to read and write the media is expensive and consumes power. Since portable computers are battery powered, use of floppy disk drive is prohibitive. To compensate, portable computer manufacturers developed software cartridges which are used in place of disk drives. For the most part, cartridges used with portable computers are read only and contain program information. This limitation prevents movement of user data beyond the portable computer. A better approach is the use of a nonvolatile read/write cartridge which could provide both program storage and data storage. The nonvolatile read/write cartridge also avoids problems of different disk sizes and formats.

Both the Tag and the cartridge are well suited for a range of applications. For example, a Tag could be used as a production traveler containing information such as lot number, inspector's identification, and quality control steps. An application in the pharmaceutical industry uses the Tag to keep track of chemical concentrations in liquids. The variables are stored in the Tag and used to precisely control formulation when mixtures are produced. The machine tool indus-

ELECTRONIC TAG BLOCK DIAGRAM Figure 13



try could use the cartridge to quickly set up operations instead of involved manual entry procedures. The rugged and durable cartridge package is also ideal for the industrial automation environment. The cartridge can store programs for process control in a factory. Because of the ease in which data can be changed, process parameters could be altered and tracked automatically.

[1]Louis J. Hart and Theodore Ciobanu, "Lithium Batteries for Memory Backup—An Evaluation Program at IBM," published in *Batteries Today*, Summer 1984 issue.

Dallas Semiconductor
SmartSocket—SmartWatch

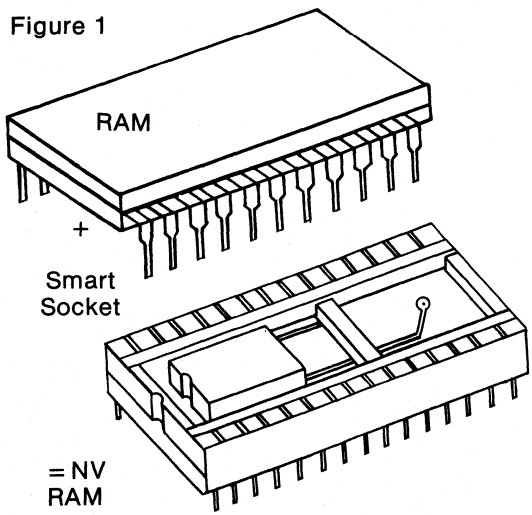
Application Note-3

SMARTSOCKET-SMARTWATCH

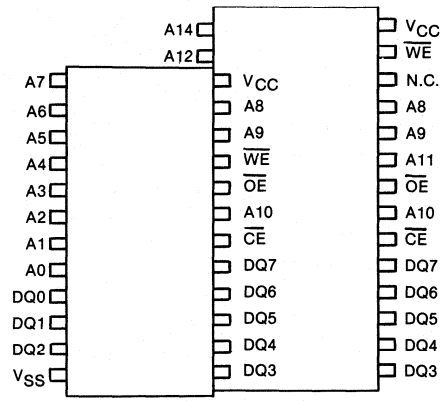
The production rate of CMOS static RAM has become staggering. Millions of units are used each year in systems that require the ideal characteristics and low cost attributed to CMOS static RAM. Now its one drawback, volatility, can be overcome by mating a standard CMOS static RAM with a DS1213 SmartSocket (Figure 1). Contained in the SmartSocket is intelligent control circuitry and a back-up lithium energy source to permanently power the mated RAM, thereby providing data retention in the absence of power. In this way the same high volume production efficiency which has made static RAM so economical can be used to make a nonvolatile RAM. Furthermore the SmartSocket accepts either 2K x 8 or 8K x 8 devices today and 32K x 8 when they become available (estimate 1986) making system design extremely flexible.

The SmartSocket conforms to the JEDEC Bytewide standard for dual in line memory (Figure 2). The identical footprint allows existing sockets to be replaced with SmartSockets thus giving a system the advantage of nonvolatile RAM without redesign. Its physical size is the same as conventional sockets except for an additional height of 0.2 inches needed for mechanical considerations.

Figure 1



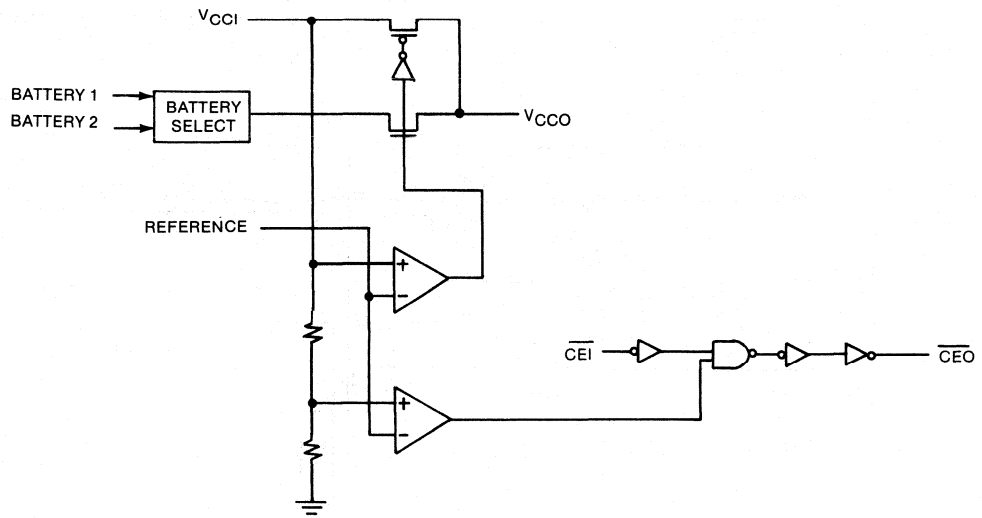
BYTEWIDE JEDEC PINOUT Figure 2



SMARTSOCKET OPERATION

The heart of the DS1213 SmartSocket is the intelligent control circuit designed by Dallas Semiconductor to perform five circuit functions required to battery back-up a CMOS memory (Figure 3). First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartSocket provides is power fail detection. Power fail detection occurs between 4.75 and 4.5 volts. The DS1213 constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable (Figure 4). The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of V_{CC} or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the

SIMPLIFIED BLOCK DIAGRAM OF THE DS1213 CONTROLLER CHIP Figure 3



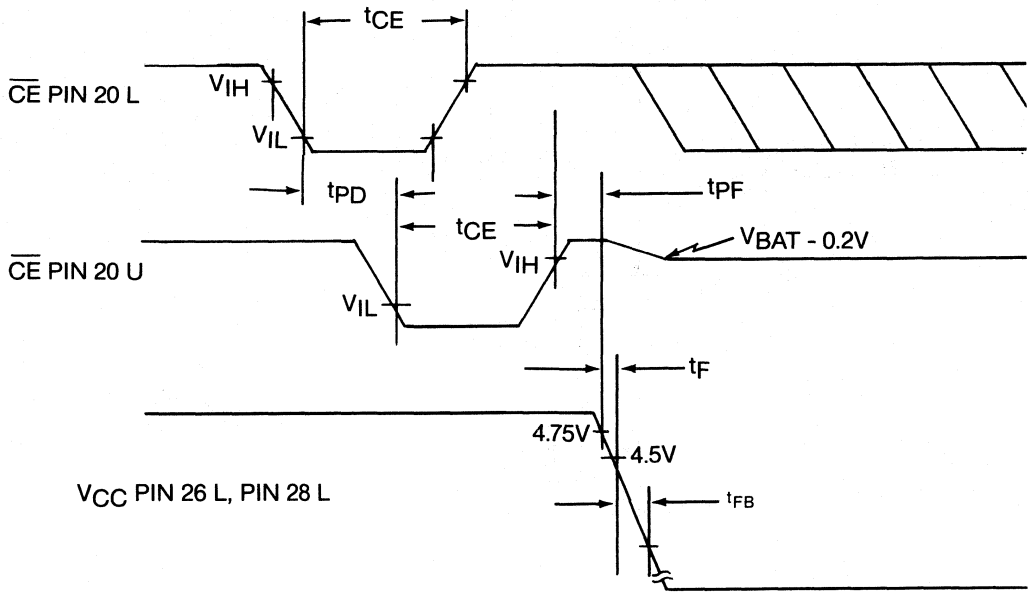
socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213 performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location,altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function which the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to insure reliability. The DS1213 SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery back up time the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

ENERGY SOURCE

The energy source within the SmartSocket is an extremely stable electrochemical system made up of a lithium anode and polycarbon monofluoride cathode. This energy system has the capacity and shelf life needed to retain data for well over 10 years in the absence of external power when mated with an appropriate CMOS static RAM (Table 1).

The lithium energy source has raised concern about reliability and has been the object of much study[1]. Data taken on the energy source used in the SmartSocket indicates a failure rate less than 0.5% per three million device hours at 70 °C.

TIMING DIAGRAM — POWER DOWN Figure 4



TIMING DIAGRAM — POWER UP

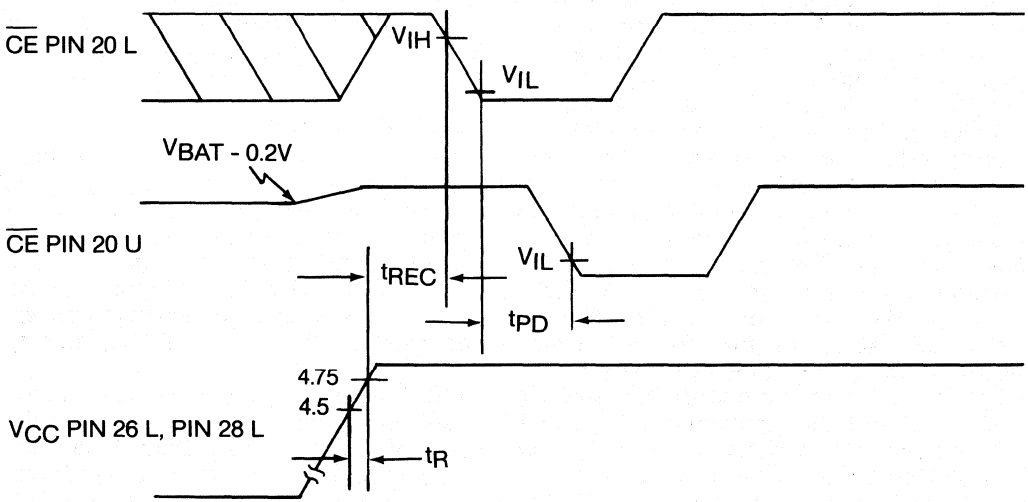


Table I

- Acceptable RAM Choices*

	2K x 8	8K x 8
Toshiba	TC5517	TC5564
NEC	uPD446	uPD4464
OKI	MSM5128	
Fujitsu	MB8416	

* 10 Years Data Retention in the Absence of Power

ADDING A TIME FUNCTION

A similar second device called the DS1216 SmartWatch retains the nonvolatile RAM capability of the SmartSocket and adds a calendar time function. The SmartWatch maintains time information including hundredths of seconds, seconds, minutes, hours, day, date, month and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. Hours of the day can be tracked in both the 12 and 24 hour format.

The value of adding a clock function to the SmartSocket lies in the amortization of the energy source with additional space saving benefits. The DS1216 SmartWatch includes the quartz crystal and circuits needed for time keeping within the same package as the SmartSocket while remaining compatible with the JEDEC Bytewide memory pinout.

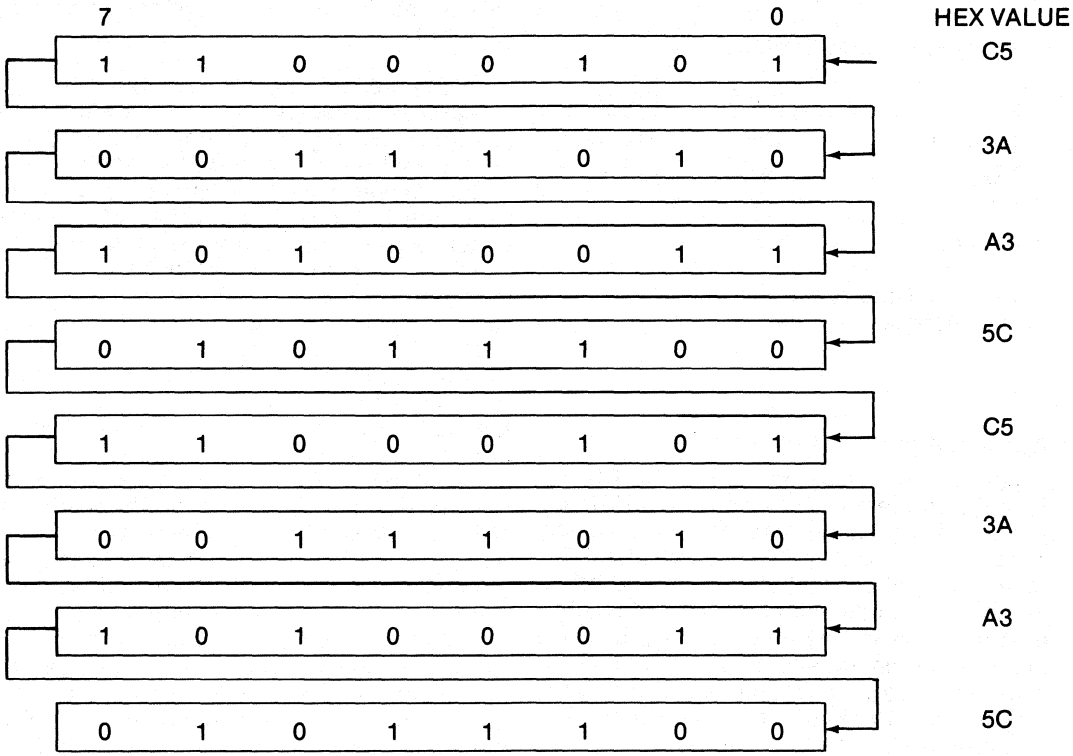
OPERATION

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64 bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch; memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CE}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch, therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 1 of the 64 bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 5). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 5



NOTE: The pattern recognition in hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64 bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 6.

Data contained in the SmartWatch registers are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12 or 24 hour mode select bit. When high, the 12 hour mode is selected. In the 12 hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24 hour mode, bit 5 is the second 10 hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator function. Bit 4 controls the reset (pin 1). When the reset bit is set to logical 1, the reset input pin is ignored. When the reset bit is set to logical 0, a low input on the reset pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

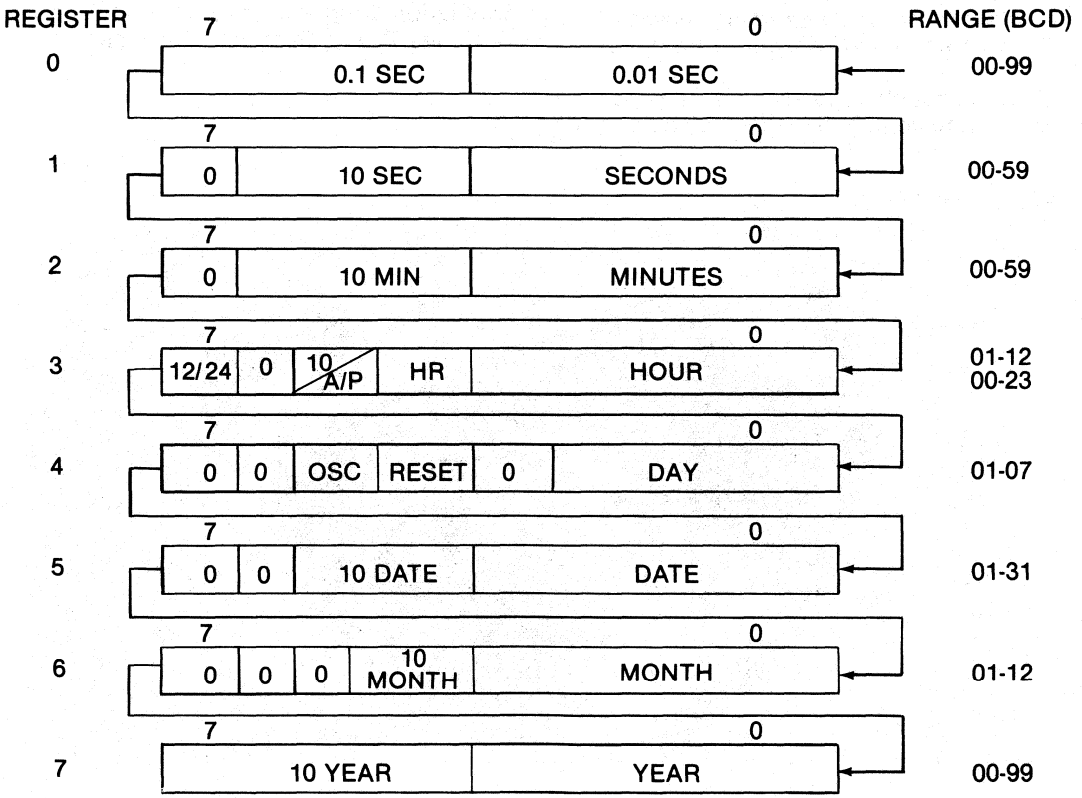
ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

HARDWARE RETROFIT

The method by which the time function of the SmartWatch is accessed allows for retrofitting existing designs which use a 28 pin bytewide socket. The hardware design is left intact, and only a software change is required to add a calendar feature to previously designed systems. Moreover, most sys-

SMARTWATCH REGISTER DEFINITION Figure 6



tems only require time information on power up since time is kept track of by the operating system while power is applied. In these applications, the software overhead is reduced to an algorithm which is executed only when the machine is turned on.

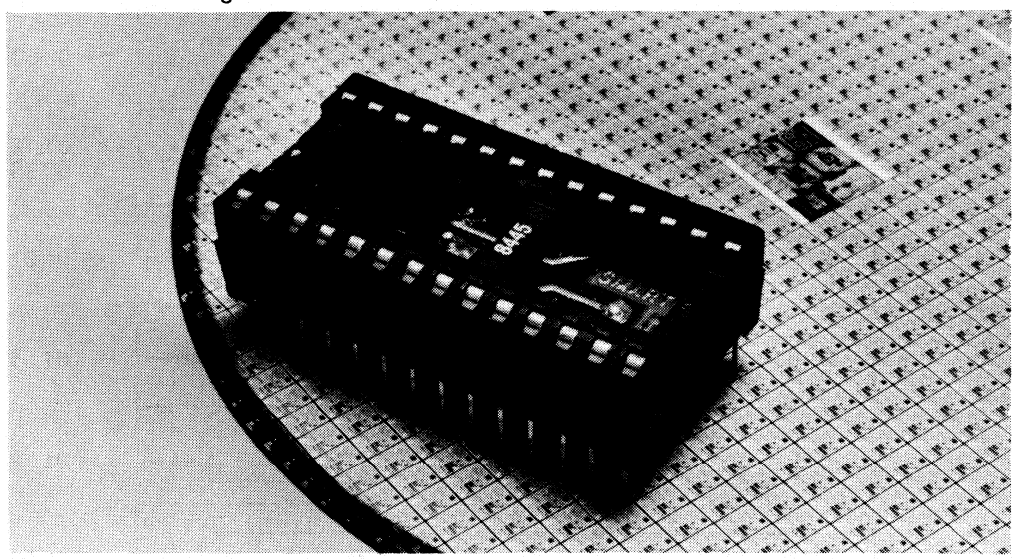
SOFTWARE

The software needed to cause entry and update for the SmartWatch consists of three subroutines (Table 2). The first, called "PATTREC," will wake up the SmartWatch and get it ready for reading and writing. After pattern recognition has been established one of two subroutines is used to either extract information or update the SmartWatch. The "WRWATCH" routine will write the 8 watch registers of the SmartWatch. The "RDWATCH" will extract information from the SmartWatch. The example shown in Table 2 is written in 8086 assembly language.

The SmartSocket replaces as many as a dozen discrete components needed to implement battery backup for a static RAM (Figure 7). Furthermore, the special control circuit techniques employed in the SmartSocket do not have the drawbacks of the earlier discrete component approach saving printed circuit board area and reducing current consumption from the battery. Manufacturing procedures are simplified by not having to deal with special handling procedures needed to avoid discharging the battery. Reliability is also greatly improved by eliminating battery clips. The SmartWatch goes further by adding a time function without increasing space requirements. Often an entire printed circuit board is used to provide this function.

[1]Louis J. Hart and Theodore Ciobanu, "Lithium Batteries for Memory Backup—An Evaluation Program at IBM," published in *Batteries Today*, Summer 1984 issue.

SMARTSOCKET Figure 7



SMARTWATCH SOFTWARE Table 2

```
;
;               SET SSSS TO THE SEGMENT OF MEMORY WHERE
;               THE SMARTWATCH WILL BE ACCESSED
;
SWATCH          SEGMENT AT SSSS
;
;               SET OOOO TO THE OFFSET OF THE SCRATCH MEMORY
;               BYTE USED TO COMMUNICATE WITH THE SMARTWATCH
;
SCRATCH         EQU     OOOO
;
SWATCH          ENDS
;
CSEG            SEGMENT PARA PUBLIC 'CODE'
                ASSUME  CS:CSEG,DS:CSEG
;
PAT             DB      0C5H,03AH,0A3H,05CH,0C5H,03AH,0A3H,05CH
;
DTA             DB      0,0,0,0,0,0,0,0
;
PATREC          PROC    NEAR
                PUSH    ES                      ;SAVE ES
                MOV     AX,SEG SWATCH           ;SET ES TO
                MOV     ES,AX                   ; SEGMENT OF SCRATCH
                MOV     CX,64                   ;DO 64 BITS
                MOV     SI,OFFSET PAT           ;SET INDEX TO PATTERN RECOGNITION
                MOV     DI,OFFSET SCRATCH
PR1:            TEST    CX,7                    ;LOAD NEXT BYTE?
                JNZ     PR2                     ;NO!
                LODSB                           ;GET NEXT PATTERN BYTE
PR2:            MOV     ES:[DI],AL              ;WRITE D0
                SHR     AL,1                    ;PREPARE NEXT DATA BIT
                LOOP    PR1                     ;LOOP BACK
                POP     ES                      ;RESTORE ES
                RET                             ;RETURN
PATREC          ENDP
;
WRWATCH         PROC    NEAR
                PUSH    ES                      ;SAVE ES
                MOV     AX,SEG SWATCH           ;SET ES TO
                MOV       ES,AX     ; SEGMENT OF SCRATCH
                MOV       CX,64     ;DO 64 BITS
                MOV     SI,OFFSET DTA           ;SET INDEX TO DATA
                MOV     DI,OFFSET SCRATCH
WW1:            TEST    CX,7                    ;GET NEXT BYTE?
                JNZ     WW2                     ;NO!
                LODSB                           ;GET DATA BYTE
WW2:            MOV     ES:[DI],AL              ;WRITE D0
                SHR     AL,1                    ;PREPARE NEXT DATA BIT
                LOOP    WW1                     ;LOOP BACK
                POP     ES                      ;RESTORE ES
                RET                             ;RETURN
WRWATCH         ENDP
```

```
;
RDWATCH   PROC    NEAR
          PUSH    DS                  ;SAVE DS
          MOV     AX,SEG SWATCH       ;SET DS TO
          MOV     DS,AX               ; SEGMENT OF SCRATCH
          MOV     CX,64               ;DO 64 BITS
          MOV     SI,OFFSET SCRATCH
          MOV     DI,OFFSET DTA       ;SET INDEX TO DATA
RW1:      JCXZ    RW2                 ;DONE?
          MOV     AH,[SI]             ;READ D0
          SHR     AX,1                ;PREPARE NEXT DATA BIT
          DEC     CX                  ;UPDATE COUNTER
          TEST    CX,7                ;SAVE NEXT BYTE?
          JNZ     RW1                 ;NO!
          STOSB                       ;SAVE DATA BYTE
          JMP     RW1
RW2:      POP     DS                  ;RESTORE DS
          RET                         ;RETURN
RDWATCH   ENDP
;
CSEG      ENDS
          END
```

Dallas Semiconductor
DS1213B SmartSocket Options

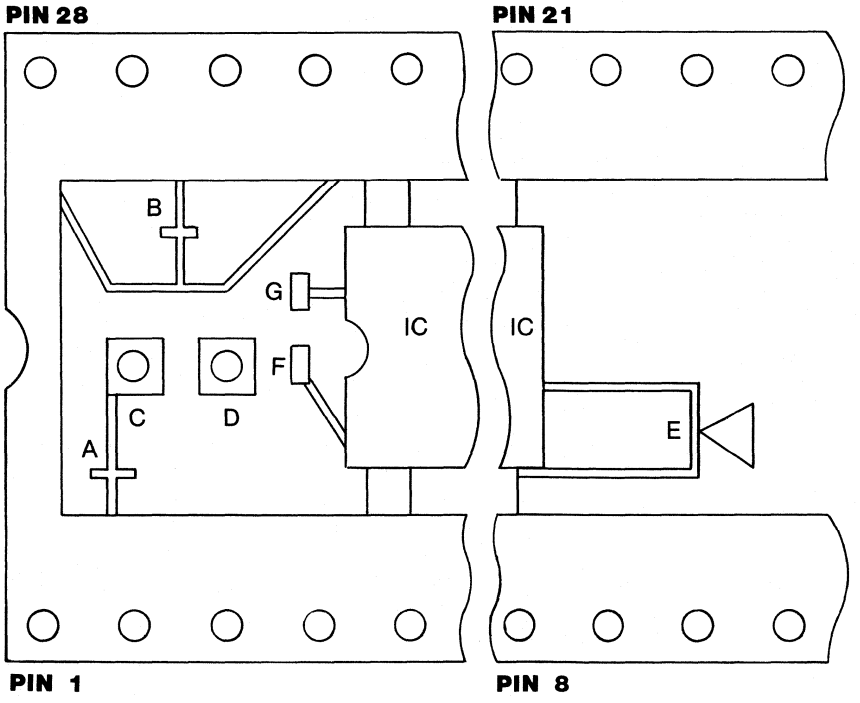
Application Note-4

DS1213B SMARTSOCKET OPTIONS

The DS1213B SmartSocket is capable of supporting two user implemented modifications. One is to suport 32K x 8 RAM operation by disconnecting pin 26 from V_{CC} and reconnecting it as a pass-through pin. The other modification would change the nonvolatile controller operation from a 5% (4.75V) to a 10% (4.50V) write protect trip point. Refer to the drawing supplied.

MODIFICATION 1: Disconnecting pin 26 from V_{CC}
STEP 1. Cut etches at locations A and B (marked with slash)
STEP 2. Jumper locations C and D (square pads)

MODIFICATION 2: 5% to 10% tolerance
STEP 1. Cut etch at location E (marked with triangle)
STEP 2. Jumper locations F and G (small rectangular pads)



Dallas Semiconductor
Integrated Battery Backup

Application Note-5

INTEGRATED BATTERY BACKUP

A CMOS chip set protects critical information in microprocessor-based systems during power loss. Called Integrated Battery Backup, the product provides for the orderly shutdown and automatic restart of processor-based systems. It is, in essence, a micro-level uninterruptable power supply. Particularly useful in industrial automation applications, Integrated Battery Backup allows a system to restart a task where it stopped as if power disruption had not occurred. By saving the data, the system picks up where it left off, thus avoiding wasted efforts and the inconvenience of re-booting.

Integrated Battery Backup is a modular chip set that can be used in its entirety or as individual components according to need. The DS1231 Power Monitor warns a processor of an impending power failure before it happens, providing time for critical data to be stored in nonvolatile memory before system power is lost. The Nonvolatile Controller/Decoder (DS1210, DS1211, DS1212, DS1221) safeguards against RAM data loss during power up and down transients. It automatically switches to battery when power failure occurs and consumes a minute battery current of less than 100 nA. The DS1260 SmartBattery supplies uninterruptable power in the absence of V_{CC} to maintain data in nonvolatile memory for more than 10 years. A supplemental function of software controlled write inhibit can be provided by the DS1234 or DS1222. The DS1215 TimeKeeper adds the capability of time stamping and dating events.

System designers can use these low-cost chips to protect critical system data and avert the chaos that accompanies unforeseeable power failures.

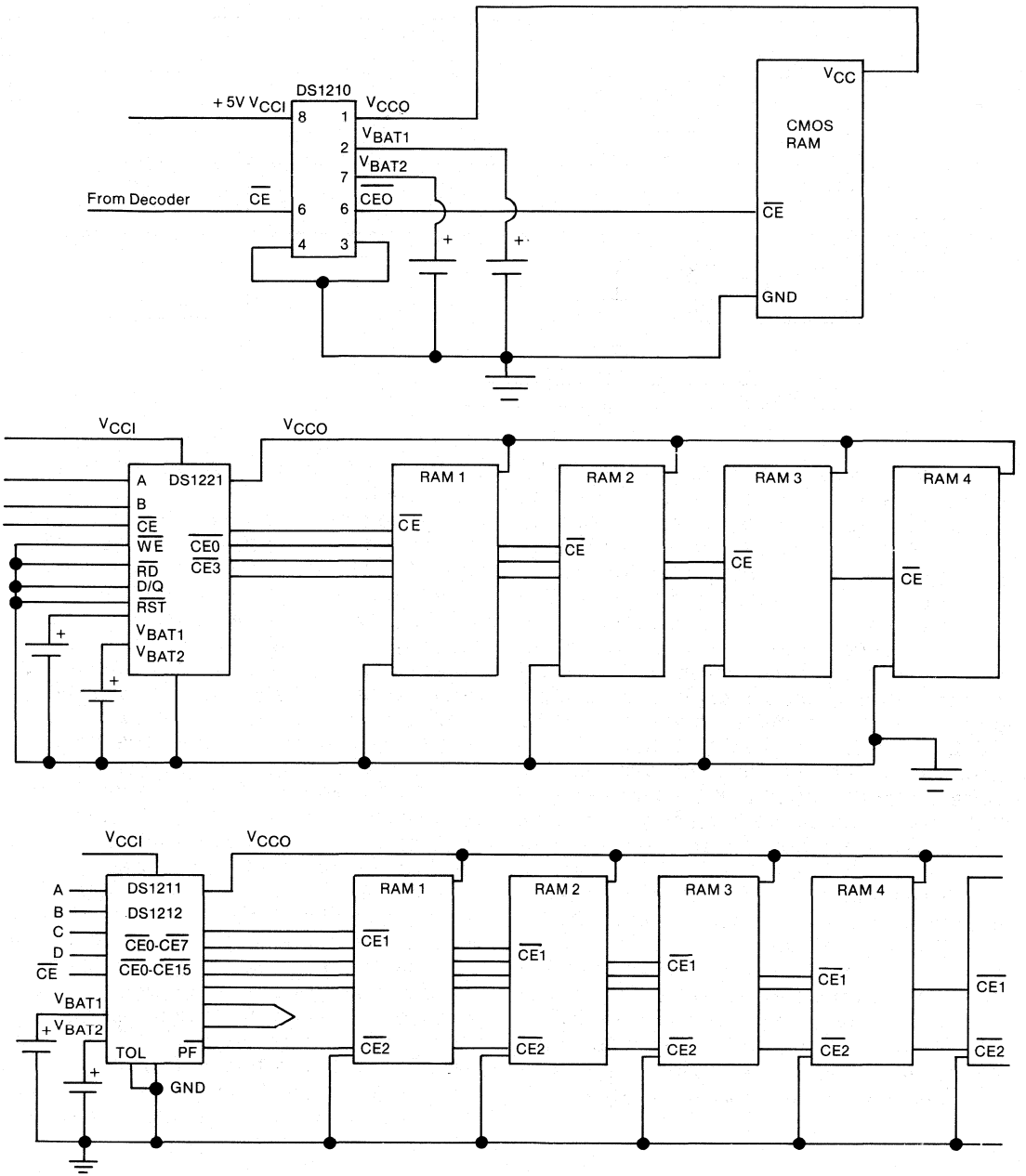
PROPER BATTERY BACKUP METHODOLOGY

A battery backup scheme which will flawlessly retain data requires a two-part strategy. The first part involves memory itself. For a memory to retain data in the absence of power, it must have a backup energy source, a switch to direct power from the main supply or the backup supply, and detection of power failure so that the memory can be write-protected during power transients. The second part of a battery backup strategy involves control of the microprocessor. The processor should be warned in advance of impending power loss so that last minute housekeeping chores can be orchestrated. As a minimum, enough warning should be provided for an orderly shutdown before power goes out of tolerance. The amount of advance warning required is a function of application. The earliest warning can be given by sensing power supply conditions on the A.C. power line or on the filter capacitor energy reservoir upstream of the regulator. This type of power sensing allows the processor to take advantage of hold up time, which is usually several milliseconds for linear supplies and tens of milliseconds for switching supplies. A power fail signal generated from the power sensing device can be used to interrupt the processor for a software-controlled shutdown routine. After the routine is executed, the processor then enters a wait state before V_{CC} (+5 volts) becomes abnormal. When V_{CC} actually goes out of tolerance, the processor is forced into a reset mode which will drive all control signals to an inactive level and put the data and address bus to a high impedance state. Processor reset prevents further activity from occurring which could disturb nonvolatile memory. Reset circuitry must be designed to clamp reset in the active state until power is restored to an in-tolerance condition and the processor's internal clocks have stabilized. A stabilization period of tens of milliseconds is required. The DS1231 Power Monitor has a built-in timer to meet this requirement.

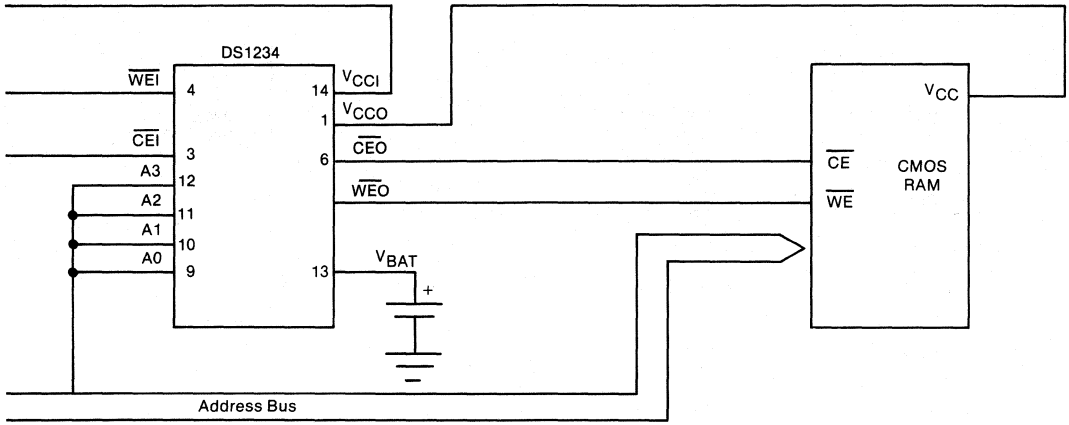
NONVOLATILE MEMORY CONTROLLER

Converting static CMOS RAM into nonvolatile memories has often been accomplished by a number of power-consuming discrete circuits. Dallas Semiconductor's nonvolatile controllers support from one to sixteen

NONVOLATILE CONTROLLERS CAN TRANSFORM FROM ONE TO SIXTEEN CMOS STATIC RAMS INTO NONVOLATILE MEMORIES Figure 1



CONDITIONAL NONVOLATILE CONTROLLER INHIBITS WRITES AND DISCONNECTS BATTERY VIA SOFTWARE Figure 2



memories. These controllers consume insignificant battery current and perform all the circuit functions required to battery backup static RAMs, including power switching, power fail detection, write protection, decoding, and optional battery redundancy. The diagrams in Figure 1 illustrate the typical hook-up between the nonvolatile controllers and memory. Each diagram shows redundant batteries. If only one battery is sufficient, the other battery pin must be grounded. The DS1210, DS1211, and DS1212 have a tolerance pin which selects either 5% or 10% write protection points on the 5-volt supply. With the tolerance pin grounded (as shown) power fail detection occurs between 4.75 volts and 4.5 volts. Power fail detection forces the chip enable outputs to memory to a high level, thereby providing write protection. The DS1221 does not have a tolerance pin and power fail detection is fixed to occur between 4.5 volts and 4.25 volts. The DS1221 has a security mode that can be used by special order from Dallas Semiconductor. When this mode is not employed, pins WE, $\overline{RD}$, D/Q, and $\overline{RST}$ must be grounded.

CONDITIONAL NONVOLATILE MEMORY CONTROLLER

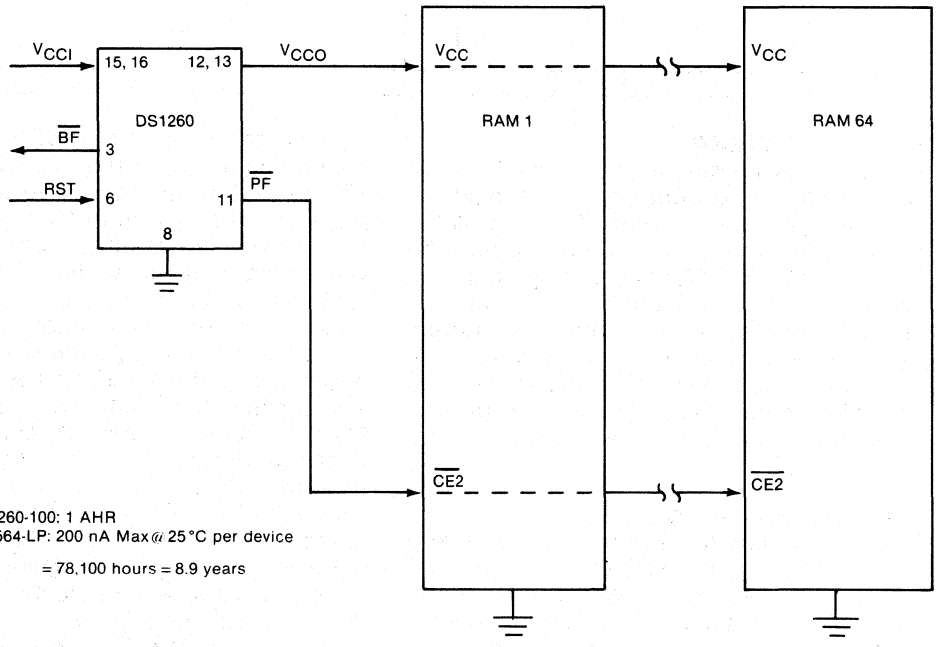
Some applications require a memory which is only written to under special conditions. The DS1234 offers an additional level of write protection for these applications by providing two software-controlled switches (see Figure 2). One switch will inhibit the writes by forcing $\overline{WEO}$ high regardless of the write enable input $\overline{WEI}$. The second switch is used to disconnect the battery, making the connected memory volatile. The switches are set by pattern recognition on address inputs A0 through A3. Pattern recognition is accomplished by presenting 16 consecutive patterns of 4 bits each on the address inputs which are strobed into the device with the chip enable signal. When the switches are set for nonvolatile operation, the DS1234 write protects connected memory via the chip enable signal by forcing the chip enable output signal ($\overline{CEO}$) to a high level when V_{CC} is out of tolerance. Read-only operation is accomplished by restricting $\overline{WEO}$ to a high level. The switch settings can be changed at any time as long as V_{CC} is within tolerance. The switches are nonvolatile as long as battery power is present.

THE SMARTBATTERY

A critical element in a battery-backed-up memory system is the battery itself. Batteries had been considered unreliable and a maintenance problem. Additional problems with battery handling and mounting have also been cited as major barriers to use. This is no longer true. Dallas Semiconductor's DS1260 SmartBattery supplies 1 amp hour of lithium energy at 3 volts and has a shelf life of more than ten years. Using the proper components and design techniques, this device can be installed in a system to last the useful life of the system. However, the device is designed to be replaceable if discharge rates are so high as to deplete the energy before the system is obsolete. For convenience it has been designed to plug into a standard 16-pin DIP socket. In addition to sourcing energy the SmartBattery incorporates a semiconductor IC to solve system problems associated with battery backup (Figure 3). The SmartBattery automatically switches power as required. Up to 250 mA of V_{CC} power can be routed through and 5 mA can be sourced from the battery when V_{CC} is less than 3 volts. The power fail signal ($\overline{PF}$) can be used to write protect memory when V_{CC} drops below 4.25 volts (typical). The battery fail signal ($\overline{BF}$) can be used to tell the processor if battery is expended. This signal reports when battery voltage is less than 2 volts.

A major concern is how to identify that a battery has full capacity, particularly when batteries are subject to uncertain handling conditions. The SmartBattery has an "electronic seal" implemented with both chip technology and special packaging to ensure absolute freshness. The reset input (RST) causes the battery supply to be disconnected from its pins so that no discharge occurs during storage, shipping and handling; therefore, battery life is maximized. Once reset, the SmartBattery is designed to remain in an off-state and then automatically reactivated when V_{CC} (+5 volts) is applied. Subsequently, the SmartBattery will become uninterruptable even if the +5 volts is removed.

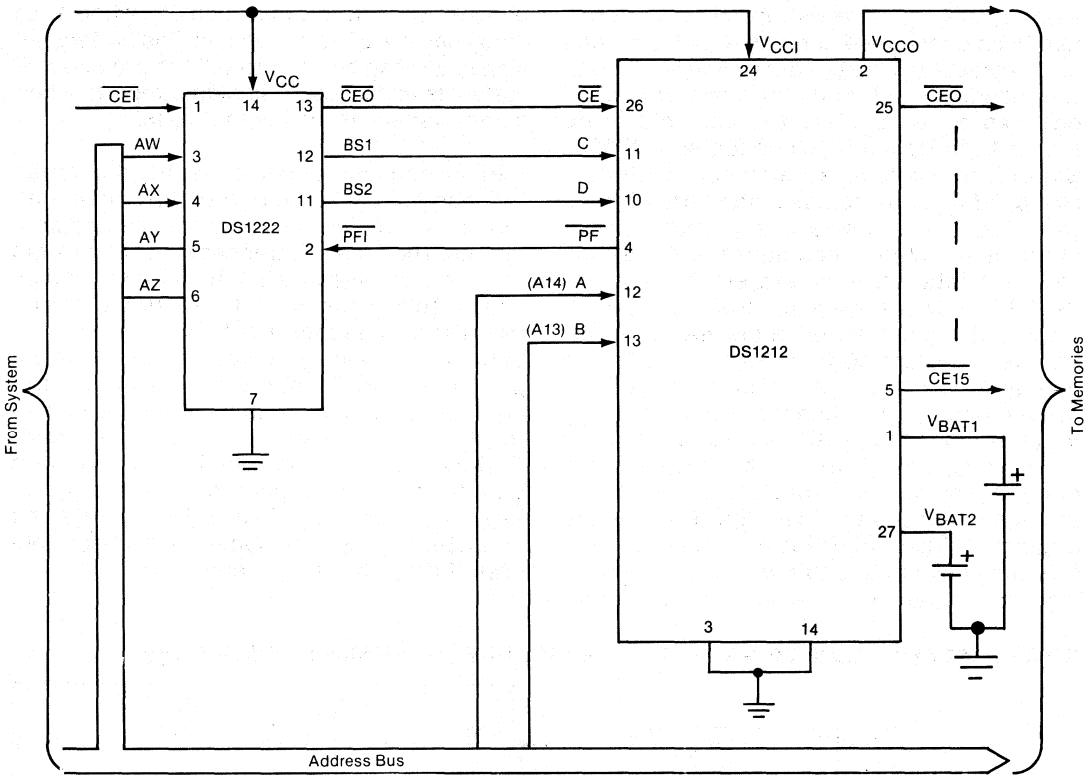
SMARTBATTERY MAINTAINS 64 8K x 8 RAMS FOR > 8 YEARS WITHOUT V_{CC} Figure 3



SmartBattery DS1260-100: 1 AHR
8K x 8 SRAM TC5564-LP: 200 nA Max @ 25°C per device

$$\frac{1}{200 \times 10^{-9} \times 64} = 78{,}100 \text{ hours} = 8.9 \text{ years}$$

BANK SWITCHING EXTENDS NONVOLATILE MEMORY SPACE Figure 4



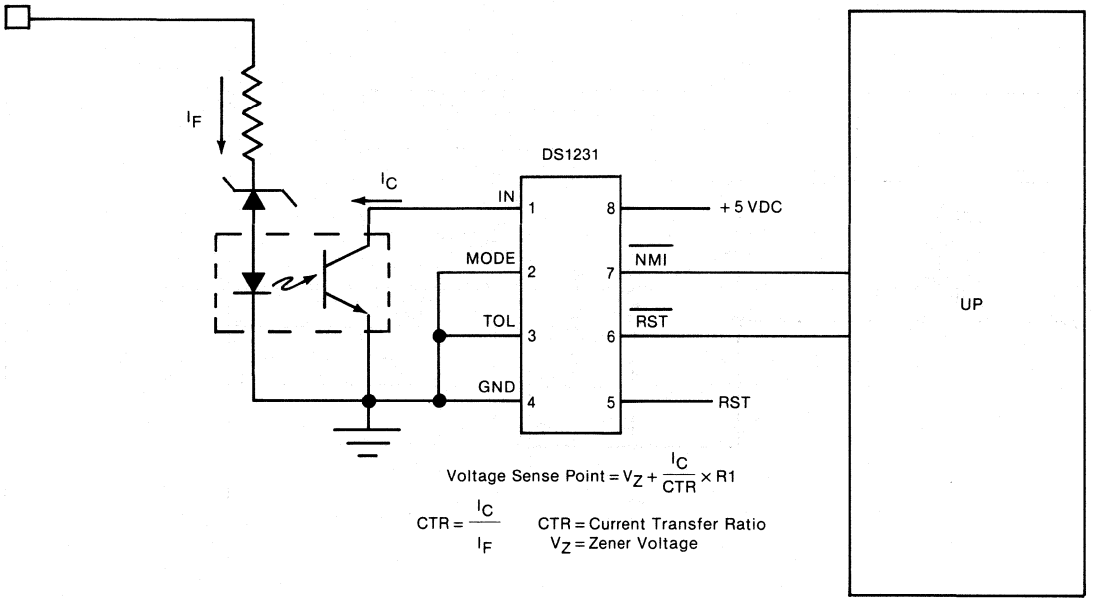
BANK SWITCHING

While bank switching is not involved in making memory nonvolatile, it does extend the processor's address map for nonvolatile memory. Figure 4 is an example of how the DS1222 and DS1212 connect together. The application, as drawn, controls four banks of 32K x 8 nonvolatile RAM. The bank switching scheme is derived from pattern recognition on four address lines. The pattern is 16 bits deep, which also adds a level of security to memory in addition to the bank switching function.

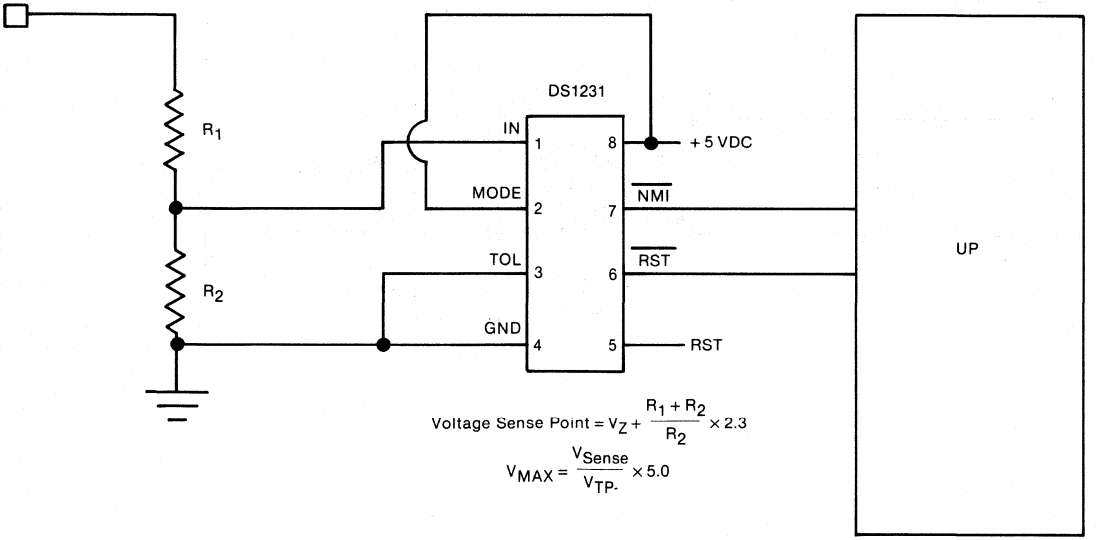
THE POWER MONITOR

As mentioned earlier, proper battery backup methodology is a two-part strategy that must be followed in order to successfully accomplish reliable nonvolatile RAM operation. So far, controlling memory has been discussed. The second half of the strategy is controlling the processor. The DS1231 Power Monitor is a device designed to control the processor through an orderly shutdown and restart associated with power failure. An advanced warning by sensing power failure as far back into the power suply as possible is critical to an orderly shutdown. Figures 5, 6, 7 and 8 show alternate methods of sensing power levels. Figures 5 and 8 show the Power Monitor in the current mode. In this mode the DS1231 is sourcing 30 *u*A to the opto-isolators through the IN pin. Figures 6 and 7 show the DS1231 in the high impedance mode where the IN pin is a high impedance input to the voltage sense point. Methods of sensing power which provide isolation are often preferred for safety reasons. However, the simple circuit of Figure 6 is adequate for many systems. The IN pin on the DS1231 pro-

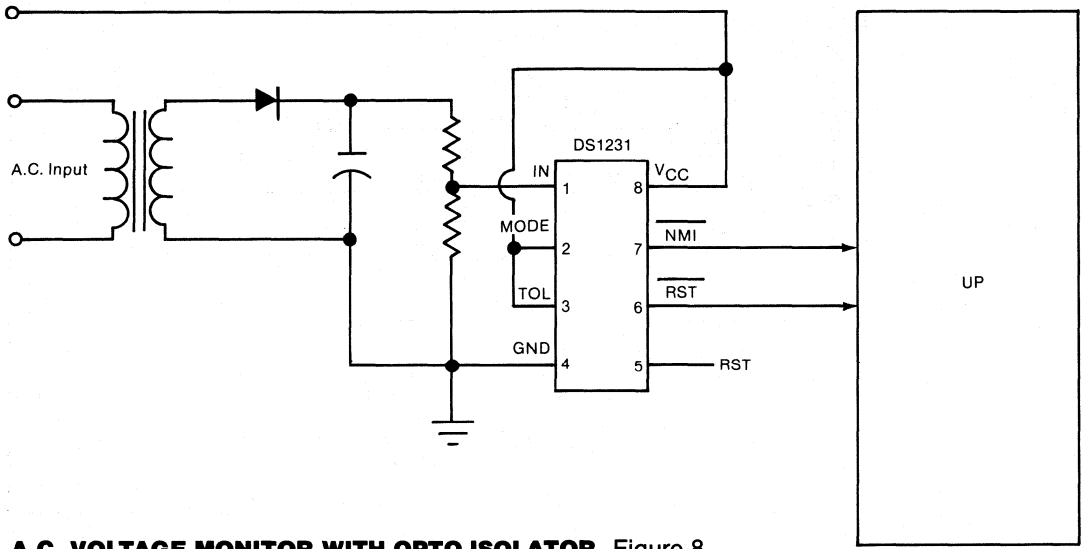
D.C. VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 5



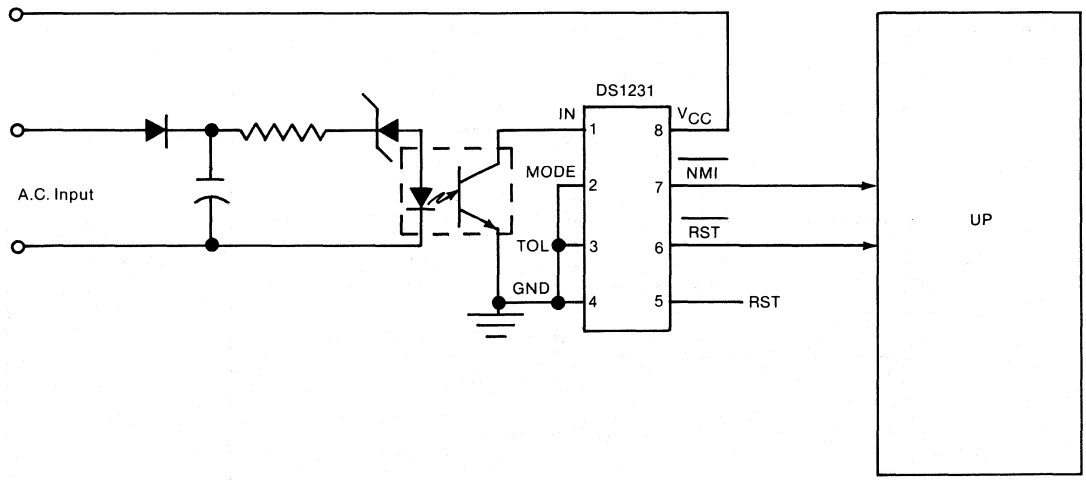
D.C. VOLTAGE MONITOR WITHOUT ISOLATION Figure 6



A.C. VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 7



A.C. VOLTAGE MONITOR WITH OPTO-ISOLATOR Figure 8



RESET CONTROL OF MICROPROCESSORS
Figure 9

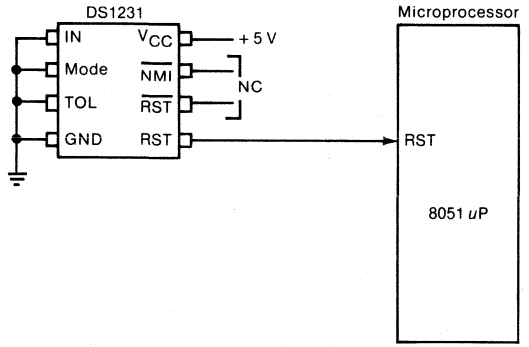
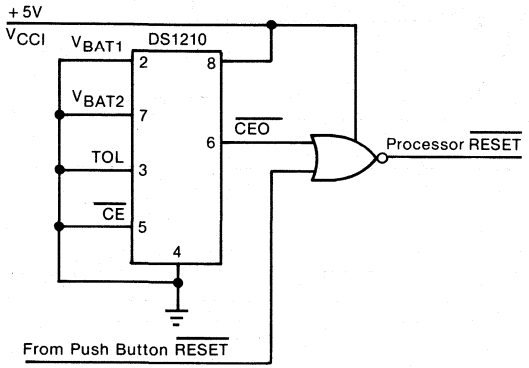


Figure 10



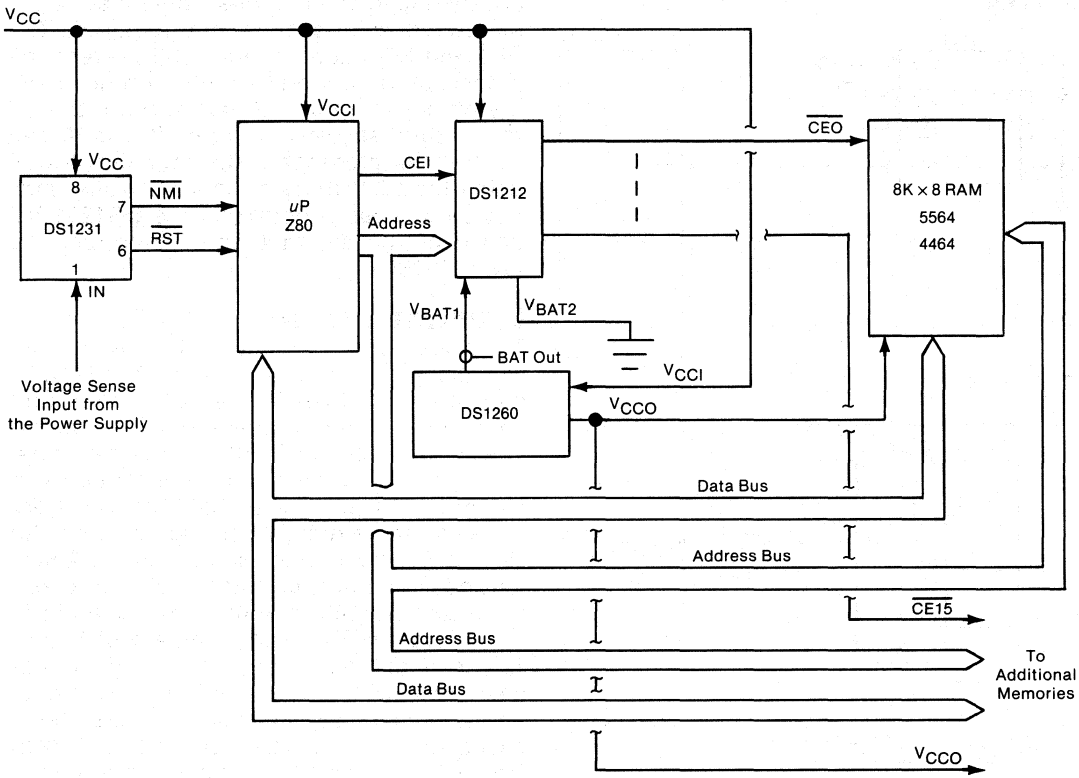
duces $\overline{NMI}$ as soon as power loss is detected. NMI, nonmaskable interrupt, is normally the highest level of interrupt in a system. Power fail software routines must be executed between the time that NMI occurs and loss of V_{CC}. As V_{CC} falls below the trip point which is set by the tolerance pin, reset ($\overline{RST}$ and RST) will go to the active state. The function of placing a processor in reset stops all activity. The DS1231 holds the $\overline{RST}$ and RST signals active until +5 volts is back to an intolerance condition and a 250 ms minimum has elapsed. The delay on power up allows the processor to stabilize before executing instructions.

Alternate methods of processor reset control are shown in Figures 9 and 10. Neither of these circuits involves early warning. This is acceptable in applications where a software controlled shutdown is not required. The $\overline{RST}$ and RST signals must still prevent the processor from inadvertently writing memory on power up and power down. Either of the circuits shown in Figures 9 and 10 can control the processor. The implementation using the DS1210 as a reset controller may not be as cost effective as the DS1231 because of the external gate to correct the level of $\overline{CEO}$.

COMPLETE SYSTEM

The block diagram of Figure 11 shows a complete nonvolatile memory system. The DS1231 provides for both software notification and hardware control of the processor during power down/up. The DS1212 is used as a decoder and nonvolatile controller for up to 16 memories. Finally the DS1260 SmartBattery sources uninterruptable power for both the DS1212 controller and the memories. A system designed in this manner can be crash proof and can retain data for the useful life of the system. The block diagram of Figure 12 has all of the capability of the circuit just described with two important additions. First, time-of-day information has been added, using a Dallas Semiconductor DS1215 TimeKeeper. Continuous power is supplied to the DS1215 via the SmartBattery. The DS1215 has the advantage of not requiring a decoder. The watch feature is accessed transparent to memory via software controlled pattern recognition similar to that described earlier for the DS1222 and DS1234. The circuit implementation adds a time stamping and dating capability at a very modest increase in cost. The final addition to this circuit is the DS1222 Bank Switch. The Bank Switch is used to selectively inhibit writes to RAM under software control. This is accomplished by routing write command signals from the processor through the DS1222. When the DS1222 is first powered on, the write command to the RAMs is blocked preventing data from being inadvertently changed. After power up write commands can be passed through at the discretion of software. The

INTEGRATED BATTERY BACKUP Figure 11



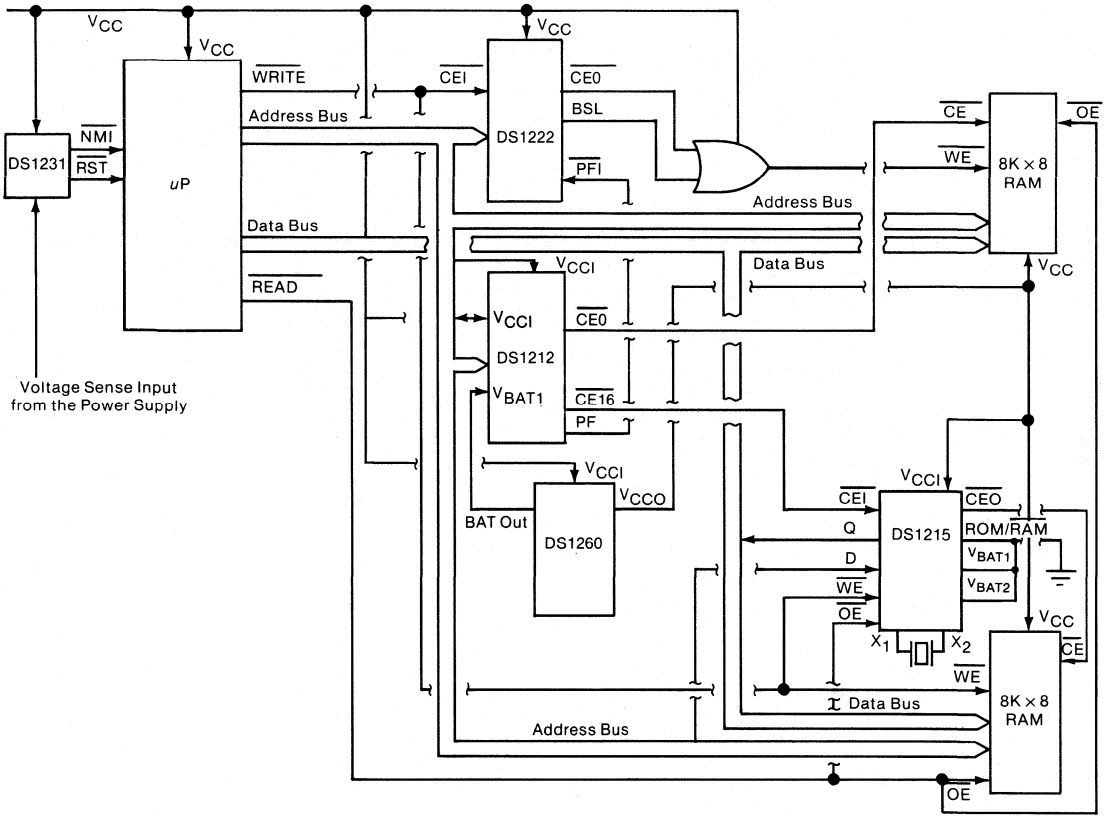
appropriate write commands can be enabled via pattern recognition on four address lines using the write strobe to gate this pattern into the DS1222. The use of the DS1222 in this manner gives an added level of write protection. A fully implemented version of this circuit supports 16 nonvolatile memories partitioned in four groups. Each group can be selectively write protected with the DS1222 circuit.

CONCLUSION

Battery backed up memory applications are increasing at a rapid pace. The principal reason for growth is the benefit accrued to the system when RAM can be made to remember. While the need for battery backup has been increasing, methodology and standard circuits to implement designs have been inadequate. In fact, many battery backup implementations lack the thoroughness to reliability protect data during power transients.

A solution to problems of battery backed up memory design is embodied in a modular product line from Dallas Semiconductor called Integrated Battery Backup. This family of products includes the Nonvolatile Controller (DS1210, DS1211, DS1212, DS1221, DS1234), SmartBattery (DS1260), Power Monitor (DS1231), Bank Switch (DS1222) and a TimeKeeper (DS1215).

INTEGRATED BATTERY BACKUP SUPPLEMENTED WITH SOFTWARE WRITE PROTECT AND TIMEKEEPING Figure 12



Dallas Semiconductor T-Carrier Chip Set

Application Note-6

T-CARRIER CHIP SET ADAPTS TO CHANGING NETWORK STANDARDS

As T1 gains mainstream acceptance as the backbone of high-speed communications, ICs that meet the timing, control and compatibility demands of T1 electronics are becoming a necessity.

The interconnection of personal computers, terminals and telephones in the business environment is experiencing explosive growth. T1 is a cost effective means of linking such automated offices, and serves as an alternative to high speed modems in the data transport environment. T1 is a high-speed digital network (1.544 MHz) developed by AT&T in the early 1960s to support long-haul pulse-code modulation (PCM) voice transmission. Although twisted-pair copper wire is the primary transmission medium, multiple T1 networks are supported by optical fiber, microwave and satellite links. T1 (also known as DS1) is the primary interface between the local telephone operating companies and long distance carriers such as MCI, LDS and AT&T. The local operating companies also utilize T1 in subscriber line carrier systems (SLC-96) to connect remote subscribers to the central office.

As the development of support ICs for T1 networks becomes a crucial design issue, three major design challenges for T1 electronics have emerged: framing and synchronization, control and status monitoring and backplane compatibility. A new chip set from Dallas Semiconductor, which consists of the DS2180 Serial T1 Transceiver and DS2176 T1 Receive Buffer, addresses all three challenges. This chip set, implemented in low-power CMOS technology, is compatible with both North American and Far East T-carrier networks. It supports a wide variety of features, including D4 framing, extended framing, bipolar eight zero substitution (B8ZS) and total transparency zero suppression modes. In addition, the DS2180 eliminates the substantial off-board logic necessary to interface to system control circuitry.

STANDARDS AND SERVICES

Many large corporations have utilized leased T1 lines for point-to-point data networks. These lines are higher speed cousins of the traditional leased-line modem networks. The nonswitched networks are often incompatible with each other and with the Bell system equipment, and are becoming increasingly obsolete.

The competitive atmosphere generated by divestiture has reduced the cost of T1 connections and has accelerated the introduction of special data services based on T1. These new switched services require equipment compatible with Bell system equipment, and offer performance superior to leased-line alternatives. Customer controlled reconfiguration (CCR) is one such service in which cost is based on the percentage of link utilization. CCR is cost effective at data rates that use 20 to 25 percent of the available T1 bandwidth.

The existing T1 network must be upgraded to handle the demands of increasing data traffic. These upgrades include full data transparency and extended framing. Transparency eliminates the data corruption caused by existing signaling and zero suppression techniques. Extended framing provides the network with a 4-kbit data channel, which is used for alarm and error-rate monitoring. The data channel lets the network police itself, providing superior line-fault analysis.

T1 networks can also be used on-site as an alternative to LANs in the office environment. Currently, two computer-to-PABX interface specifications based on T1 technology exist. The Digital Multiplexed Interfaced (DMI) standard is supported by AT&T Information Systems and Hewlett-Packard. The Computer-Peripheral-Interface (CPI) standard is backed by Northern Telecom and Digital Equipment Corp. This widespread acceptance of T1 as a prime mover of voice and data is turning it into the "RS-232" of telecommunications.

Companies developing T-carrier equipment include those specializing in PCM switching and transmission, office automation, modem and communications networks and private automatic branch exchanges (PABX) with data capability.

FRAMING AND SYNCHRONIZATION

The first challenge in designing ICs for T1 is framing and synchronization. In the Dallas Semiconductor chip set, the DS2180 transceiver handles these functions. It supports extended framing, D4 framing and derivatives of D4, such as SLC-96. In addition, features such as bit 7 stuffing (a zero suppression technique), bipolar eight zero substitution (B8ZS) and total transparency zero suppression modes are included in the device. The transceiver has autonomous transmit and receive sides. An on-board serial port links the device to a host microprocessor/microcontroller for supervision and control.

The transmit side of the DS2180 is made up of six major functional blocks: a timing and clock generator, a yellow alarm circuit, an F-bit data section (F-bit refers to the first bit transmitted), a cyclic redundancy check (CRC) section and a data selector bipolar coder. The timing and clock-generation circuit develops all on-chip and output clocks from three signal inputs (TCLK, TFSYNC and TMSYNC). The output clocks identify robbed-bit signaling (which indicates the telephone on/off-hook status) and link-data frames, making them useful for data conditioning and decoding. The rising edge of the sync inputs must be aligned with the transmit clock. Data inputs are sampled on the falling edge of the clock signal, while updated outputs occur on the rising edge. The timing inputs on the transmit side may be slaved to receive side outputs for use in drop-and-insert applications. This timing sequence is compatible with most combo-codecs.

The yellow alarm circuitry generates mode-dependent alarms for transmission into the network. The F-bit data block develops the synchronization pattern that is embedded in the outgoing data stream. The CRC circuitry subsection produces check-sum codes that are utilized in extended framing. These three subsections feed into the data selector, which builds the outgoing serial data stream via bit selection and insertion. The bipolar coder reformats the data selector output into an alternative mark inversion (AMI) format and inserts the selected zero suppression techniques. The bipolar coder also supports an on-chip loopback feature.

The heart of the receiver is the synchronizer/sync monitor, which monitors the incoming data stream for loss of frame or multiframe alignment, and searches for new alignment when synchronization loss is detected. The synchronizer uses a sophisticated, memory-intensive frame-search algorithm. Unlike earlier devices, this algorithm displays no sensitivities to emulators of the framing pattern sequence, such as digital milliwatt. It also rejects randomly induced patterns generated by network testing equipment that mimic synchronization patterns.

The Receive Control Register allows the user to tailor the characteristics of the sync algorithm to unique applications. Typical synchronization times are 4 ms (D4 framing) and 8 ms (extended framing). The resynchronization sequence occurs off-line. (The receive output timing "rolls" at the "old" alignment until the sync search is completed.) When the new frame and multiframe alignments are identified, the output timing set is jammed to the timing position of the next multi-frame boundary. When synchronization is established, the synchronizer is disabled to save power.

The output timing on the receive side is identical to the transmit timing; the bipolar decoder, yellow alarm detector and CRC circuitry are complements of those blocks used on the transmit side of the device. Alarm conditions detected on the receive side (loss of synchronization, carrier loss, framing error) appear as outputs and are reported to the status and error-count registers. The Receive Mark Register allows idle or digital milliwatt codes to be selectively inserted over incoming channels. This feature can be used in channel-unit applications for channel-level adjustment and field service.

CONTROL AND STATUS MONITORING

A major disadvantage of most first-generation transceivers is that they require substantial off-board logic to interface to system control, or they support rigid control protocols which limit the host control options of the designer. The DS2180's on-board serial port utilizes a simple synchronous protocol and interfaces directly to popular microprocessors/microcontrollers, such as the 8051. Sixteen registers establish the device's operating characteristics and report error status and alarm conditions. This flexible control architecture eliminates support hardware and minimizes processor overhead.

The read/write timing for the port used to access the registers is independent of the transmit and receive timing. This read/write timing is compatible with the 8051 on-board serial port operating in mode 0. With a master clock of 12 MHz, the 8051 can write or read a single register in less than 25 *us*. In addition, a burst mode allows all registers to be consecutively read or written.

The basic operational control characteristics of the transceiver are established by the Common Control, Transmit Control and Receive Control Registers (CCR, TCR and RCR). The CCR establishes frame, zero suppression and yellow alarm modes. A local loopback, which internally ties the transmit clock and data outputs to the receive clock and data inputs, is also enabled by the CCR. The TCR supports blue (unframed "I's") and yellow alarm transmission. Robbed-bit signaling and D4 framing insertion modes are also selected by the TCR. The RCR establishes synchronizer characteristics and selects the code word type that may be inserted in each outgoing channel.

Three other register sets are used to eliminate the off-chip control hardware that is used in existing designs. The Transmit Idle Register (TIR) allows the user to insert an idle code sequence into any outgoing channel data. The Transmit Transparency Registers (TTR) are used to disable robbed-bit signaling insertion and bit seven zero suppression on a per-channel basis. The Receive Mark Registers (RMR) replace selected incoming DS0 channels with a digital milliwatt or idle code (as selected by the RCR).

Status monitoring is handled by the Receive Status Register, which reports alarm conditions, such as a loss of synchronization, yellow alarm, carrier loss, blue alarm and error-count saturation. Unless disabled by the Receive Mask Register, any one of these events will generate an interrupt. On-board error event counters allow the device to log error events, such as bipolar violations and frame bit errors. When the error counters exceed a preprogrammed threshold, they will also generate an interrupt (unless masked). This logging capability eliminates the need for off-chip error counting logic and minimizes processor overhead. Error-event service routines may be poll or interrupt-based, depending on the system requirements.

The DS2180 also has the ability to operate in hardware mode. For preliminary system prototyping or for applications which do not require serial port features, the transceiver may be reconfigured into a hardware mode. This disables the port, clears all internal registers and redefines all serial port pins as mode control inputs. This mode allows device retrofit into existing applications where mode control and alarm conditioning are performed with discrete logic. The mode control inputs establish device framing, zero suppression, alarm and F-bit insertion characteristics.

BACKPLANE COMPATIBILITY

The Dallas Semiconductor DS2176 T1 Receive Buffer is the first T-carrier product which lets the user link transceivers to a variety of system backplanes. The DS2176 compensates for jitter and wander in the receive clock, serves as a rate buffer for backplane frequencies other than 1.544 MHz, interfaces directly to serial or parallel backplanes and supervises robbed-bit signaling.

Although the received T1 data stream averages 1.544 MHz, the data displays significant high-frequency jitter and low-frequency wander. These characteristics result from

the less-than-perfect transmission characteristics of a repeated T1 span line. An elastic store, based on first-in, first-out (FIFO) memories and discrete contention logic, is required to interface transceivers to system backplanes.

The DS2176 uses an on-chip PCM buffer to synchronize incoming data to system backplane frequencies, eliminating the need for the elastic store. The buffer depth is two frames (386 bits), which is more than adequate for most applications in which short-term jitter and wander compensation is required. This buffer "slips" whenever it is completely emptied or filled, recentering its depth to one frame. (The buffer can also be externally recentered.) Slip occurrences are reported at the SLIP output. In addition, a set of signals (System Multiframe Sync and Receive Multiframe Sync) can be used to monitor buffer depth in real time.

SIGNALING SUPERVISION

Signaling data embedded in the PCM data stream is extracted and output by the DS2176. The signaling buffer in the DS2176 allows the device to freeze the signaling outputs during slip or alarm conditions. This meets the Bell system requirements for prohibiting updates when sync or carrier signals are lost.

Signaling integration is another important feature of the DS2176. When selected, it minimizes the impact of random noise on the signaling information. For signaling integration, the channel signaling data must be in the same state for two or more multiframes before being updated at the signaling outputs. For the DS2176, two inputs are used to select the degree of integration or totally bypass the feature. The processed signaling data is not re-merged with the outgoing channel word. This maintains data integrity in mixed voice-data or data-only environments.■

A T1 TUTORIAL

T1 transmission is based on twisted pair wiring, with separate pairs used for the transmit and receive sides. T1 links require a repeater circuit every 6,000 feet to regenerate the attenuated signal; an "office repeater" is required when a loop terminates into station electronics. Higher rate transmission systems based on optical fibers are gaining widespread use. DS3 is one such system; at 45 MHz, it is made up of 28 T1 (DS1) lines.

In T1, data is transmitted in an alternate mark inversion (AMI) format, which allows clock signals to be derived from data, eliminating the need for separate clock transmission. The clock signal is extracted from the AMI waveform using phase-locked loops or LC tank circuitry. Clock extraction circuitry requires a minimum density of "1's" to operate correctly. To meet this density requirement—networks cannot transmit a code consisting solely of zeros—existing T-carrier equipment changes bit 7 of any channel consisting solely of "0's" to 1. Bit 7 stuffing does not affect the quality of voice transmission, but it does corrupt data significantly. An alternative to bit 7 stuffing is bipolar eight zero substitution (B8ZS), which replaces any transmitted zero octet with a B8ZS code word. If the last "1" transmitted was positive, the inserted word is 000 + -0- + . If the last "1" transmitted was negative, the code word inserted is 000- + 0- + . Bipolar violations occur in the fourth and seventh bit positions, but these are ignored by the receive alarm circuitry when B8ZS is enabled. The receive side detects the code word and replaces it with all zeros.

Framing refers to the format for data signaling, alarm and synchronization information on the T1 trunk. A frame of data is made up of 193 bits, and is transmitted every 125 *u*s. The first bit transmitted is known as the F-bit. The F-bit position is used for synchronization, alarm and network data link. The F-bit is followed by 24 voice or data channels, each channel being eight bits wide. These channels (known as DS0 channels) each have a data rate of 64 kbits/s.

Multiple frames make up a superframe (multiframe). One Extended Superframe consists of 24 frames. Twelve frames make up one D4 superframe.

Signaling information (telephone on-hook/off-hook status, known as robbed-bit signaling) is written over the least significant bit (LSB) of each channel every six frames. Newer systems avoid this type of data corruption by moving all signaling information to a separate DS0 channel. The use of common-channel signaling and newer zero suppression techniques such as B8ZS enhance the network's ability to carry data. This capability is known as "clear channel."■

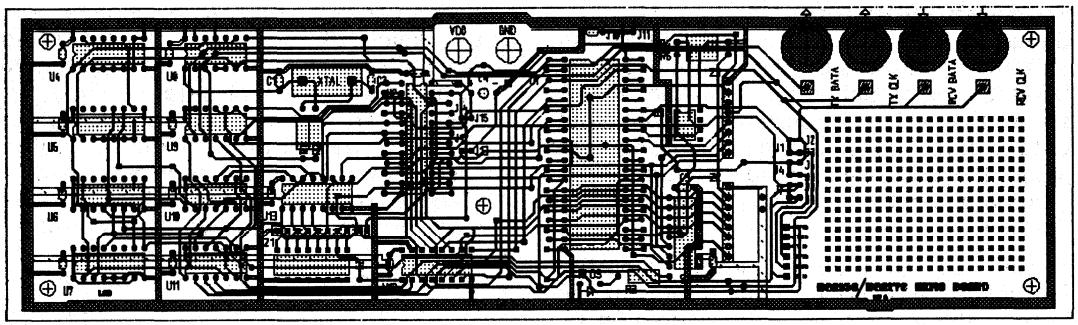
DS2180/2176 DEMO KIT

Potential users of the Dallas Semiconductor T-Carrier Chip Set may wish to purchase a DS2180/DS2176 demo kit.

The demo kit includes: samples of the DS2180 and DS2176, a small printed circuit board, logic to generate transmit side clocks, and support documentation. The kit accelerates device evaluation and system design and may be used stand-alone (hardware mode) or with software development tools (serial port mode) of the user's choice.

Device timing set and interconnect may be altered by the user to emulate end applications. A small wire-wrap area on the board allows the user to build up appropriate line interfaces, customize control logic, etc.

Demo board shown approximately one-half actual size.



Dallas Semiconductor
DS2180 Supervisory Software

Application Note-7

INTERFACING THE DS2180 T1 TRANSCEIVER TO 8051/31 MICROCONTROLLERS

This application note provides users of the DS2180 T1 Transceiver with some 8051 software examples. All of the software presented makes use of the serial control port of the DS2180, which allows access to 16 internal registers devoted to device control, configuration and status monitoring. The serial port consists of 5 pins: SDI, SDO (serial data in and out), SCLK (serial data clock in), $\overline{CS}$ (chip select) and $\overline{INT}$ (interrupt output). Although the port is very general-purpose, this application note concentrates on interfacing specifically with an 8051 processor. When configured in mode 0, the serial port of the 8051 mates perfectly with the serial port of the DS2180, requiring no external logic. This circuit hook-up is shown in Figure 1.

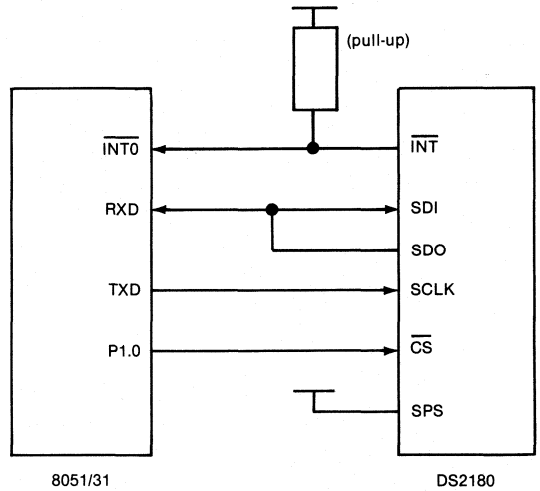
Circuit operation is very straightforward. RXD on the 8051 is a bi-directional serial bus for data in and out of the part. The TXD pin provides a serial data clock to the DS2180, allowing the transceiver to sample data on rising clock edges. A normal port pin (P1.0) enables the DS2180's port by transitioning low. The remaining connection, INT0, processes interrupt requests from the DS2180's $\overline{INT}$ output. Because this output is open-collector, a resistor pull-up is necessary to define the high state. Use of the $\overline{INT}$ output is strictly up to the user and usually depends on whether processor control is polled or interrupt-based.

Speed through the port can be very rapid and is determined by the processor internal clock. For example, if the 8051 is running at 12 MHz, then the serial clock output at TXD will be 1 MHz (a ÷ 12 of the master clock), which leads to typical read/write times of less than 25 *u*sec. Because of the $\overline{CS}$ input, several DS2180s can be supervised by the same processor by tying the clock and data lines together, and selecting each DS2180 by its $\overline{CS}$ input.

The first two software examples concentrate on how to transfer data between the 8051 and the DS2180 using the serial port. Both methods of transfer—burst and random—are supported. (Burst mode means all registers are accessed consecutively, while random mode means accessing one specific register.) The third and last example shows how DS2180-generated interrupts might be handled, specifically those interrupts caused by on-chip counter saturations. This software is useful when the user is building code to calculate BERs (bit-error-rate) for bipolar violations, CRC-6 checksum errors, loss-of-sync occurrences (OOFs) etc. Note that the software using the DS2180 internal counters obsoletes the need for external error count logic, reducing board area and cost.

Finally, this software is not meant to be a stand-alone program: it simply illustrates subroutines that may be incorporated into a larger program.

DS2180/8051 SUGGESTED HOOK-UP
Figure 1



SERIAL PORT READ ROUTINES Example 1
Purpose: Read registers from the 2180 via the serial port

Arguments: Burst mode
RO Count of bytes to receive (16)
DPTR External memory location

Random Access mode
R1 T1 register address (0-15)
ACC Data returned from DS2180

```
;
; Process burst read request
;
T1__BURST__READ:    PUSH        DPL             ;save data pointer low
                    PUSH        DPH             ;save data pointer high
                    MOV         R1,#81H         ;burst read command byte
                    SJMP        T1__RD          ;begin serial byte transfer
;
T1__RANDOM__READ:   PUSH        DPL             ;save data pointer low
                    PUSH        DPH             ;save data pointer high
                    MOV         R0,#1H          ;only 1 byte to transfer
                    MOV         DPTR,#FFFFH     ;point to dummy location
                    XCH         A,R1            ;get the T1 reg address
                    ANL         A,#0F           ;mask out invalid bits
                    RL          A               ;shift left one bit
                    ORL         A,#1H           ;indicate a read function
                    XCH         A,R1            ;....and save the result
;
; Begin reading data from the serial port (RXD, TXD)
;
T1__RD:             SETB        P1.0            ;disable DS2180
                    CLR         P1.0            ;enable DS2180
                    PUT__SERIAL__PORT R1 (write command byte)
;
T1__RLP:            GET__SERIAL__PORT A (read data byte)
                    MOVX        @DPTR,A         ;store this byte
                    INC         DPTR            ;point to next destination byte
                    DJNZ        R0,T1__RLP      ;continue until all reg done
                    SETB        P1.0            ;set DS2180 CS pin high
                    RET                         ;return to caller
```

MACRO DEFINITIONS

```
.MACRO          PUT_SERIAL_PORT         REG
                CLR         SCON.REN    ;disable serial receive
                CLR         SCON.T1     ;clear transmit done flag
                MOV         SBUF, REG   ;write serial byte
          LBL1: JNB         SCON.T1,LBL1 ;wait until transfer complete
                CLR         SCON.T1     ;clear transmit done flag

.MACRO          GET_SERIAL_PORT         REG
                SETB        SCON.REN    ;enable serial receive
                CLR         SCON.R1     ;read serial byte
          LBL2: JNB         SCON.R1,LBL2 ;wait until transfer complete
                MOV         REG,SBUF    ;fetch the byte just read
                CLR         SCON.REN    ;disable serial receive
```

SERIAL PORT WRITE ROUTINES Example 2
Purpose: Write registers to the 2180 via the serial port

```
Arguments:   Burst mode
         RO  Count of bytes to transmit (16)
       DPTR  External memory location

             Random Access mode
         R1  T1 register address (0-15)
        ACC  Data value for transfer
;
; Process burst write request
;
T1_BURST_WRITE:  PUSH        DPL         ;save data pointer low
                 PUSH        DPH         ;save data pointer high
                 PUSH        ACC         ;save caller's accumulator
                 MOV         R1,#80H     ;burst mode command byte
                 MOVX        A,@DPTR     ;get first data byte
                 SJMP        T1_WT       ;begin actual transfer
;
; Process random write request
;
T1_RANDOM_WRITE: PUSH        DPL         ;save data pointer low
                 PUSH        DPH         ;save data pointer high
                 PUSH        ACC         ;save caller's accumulator
                 MOV         R0,#1H      ;only 1 byte to transfer
                 MOV         DPTR,#FFFFH ;point to dummy location
                 XCH         A,R1        ;retrieve DS2180 address
                 ANL         A,#0FH      ;mask out invalid bits
                 RL          A           ;shift left 1 bit
                 XCH         A,R1        ;....and save the result
```

```
;
; Begin writing data out to the serial port
;
T1_WT:      SETB    P1.0            ;disable DS2180
            CLR     P1.0            ;enable DS2180
            PUT_SERIAL_PORT R1 (write command byte)
;
T1_WLP:     PUT_SERIAL_PORT A (write data byte)
            INC     DPTR            ;point to next byte
            MOVX    @DPTR,A         ;store this byte
            DJNZ    R0,T1_WLP       ;continue until all reg done
            SETB    P1.0            ;disable DS2180
            RET                     ;return to caller
```

SOFTWARE FOR PROCESSING COUNTER-GENERATED INTERRUPTS FROM THE DS2180 Example 3

This routine processes interrupts on the INT0 line (Pin 12 of the 8051), generated by the $\overline{INT}$ output of the DS2180. In general any alarm bit set in the receive status register (RSR) will cause the $\overline{INT}$ pin to go low if the corresponding bit in the receive interrupt mask register (RIMR) is also set. This software example responds to interrupts generated by either a BVCS (bipolar count saturation) or an ECS (error count saturation) event. While the BVC counter is a full 8-bit counter, the ECR consists of two separate 4-bit counters in the same register. The high nibble increments on loss-of-sync occurrences and the low nibble increments on F-bit errors (the type of F-bit errors are mode-dependent). Saturation of either 4-bit counter will set the ECS bit in the RSR register.

Program flow is as follows: when an interrupt occurs, the RSR register is read to determine which counter saturated. The memory location mapping to the appropriate saturated counter is then incremented to keep a running tab of saturation occurrences. The counter in question is reloaded with a user-determined threshold before the routine returns control to the main program. This routine assumes that RIMR.7 and RIMR.6 have already been set high to allow counter-generated interrupts to occur.

```
;
; Define the external memory addresses used by this routine
;
T1_BVC_RELOAD = #0H             ;bipolar count threshold
T1_ECR_RELOAD = #1H             ;error count threshold
T1_BVC_ERRORS = #2H             ;bipolar sat count
T1_ESF_ERRORS = #3H             ;low nibble ECR sat count
T1_OOF_ERRORS = #4H             ;high nibble ECR sat count
;
; Read the T1 receive status register (RCR)
;
ERRCHK:  MOV    R1,#T1_RSR          ;load register address
         LCALL  T1_RANDOM_READ      ;read one T1 register
         JB     A.7,BVCS            ;process bipolar count sat
         JB     A.6,ECS             ;process error count sat
         SJMP   INTO_R              ;....or terminate interrupt
```

```
;
; Process a bipolar violation count saturation by first reloading the user-defined count thresh-
; old and then incrementing the running count memory location (T1_BVC_ERRORS).
;
BVCS:   MOV     DPTR,#T1_BVC_RELOAD
        MOVX    A,@DPTR             ;fetch BVC count threshold
        MOV     R1,#T1_BVCR         ;fetch BVCR address
        LCALL   T1_RANDOM_WRITE     ;write one T1 register
        MOV     DPTR,#T1_BVC_ERRORS
        MOVX    A,@DPTR             ;fetch running count
        INC     A                   ;increment count by 1
        MOVX    @DPTR,A             ;put new count back
;
; Now check for any other counter saturation
;
        SJMP    ERRCHK
;
; Process error count saturation by a similar procedure except that we must determine which
; nibble of the ECR is affected. Then only the counter saturated is reset to the user-specified
; value.
;
ECS:    MOV     R1,#T1_ECR          ;load register address
        LCALL   T1_RANDOM_READ      ;read one T1 register
        MOV     RO,A                ;store ECR count in RO
        ANL     A,#0FH              ;mask to get low nibble
        XRL     A,#0FH              ;xor to see if saturated
        JNZ     ECS_OOF             ;if not, must be high nibble
        MOV     A,RO                ;restore ECR count
        ANL     A,#F0H              ;mask to save high nibble
        MOV     RO,A                ;save high nibble
        MOV     DPTR,#T1_ECR_RELOAD
        MOVX    A,#DPTR             ;get ERC threshold value
        ANL     A,#0FH              ;mask to get low nibble
        ORL     A,RO                ;or high and low nibbles
        MOV     RO,A                ;save as new ERC count
;
; Now increment the low nibble (T1_ESF_ERRORS) running count
;
        MOV     DPTR,#T1_ESF_ERRORS
        MOVX    A,@DPTR             ;fetch ESF running count
        INC     A                   ;increment count by 1
        MOVX    @DPTR,A             ;put new count back
```

```
;
; Now check for high nibble (OOF counter) saturation and process this event similarly.
;
ECS_OOF: MOV     A,RO                    ;restore ECR count value
         ANL     A,#F0H                  ;mask to get OOF count
         XRL     A,#F0H                  ;xor to see if saturated
         JNZ     ERRCHK                  ;if not, then we are done
         MOV     A,RO                    ;restore ECR count value
         ANL     A,#0FH                  ;mask to save low nibble
         MOV     RO,A                    ;save low nibble
         MOV     DPTR,#T1_ECR_RELOAD
         MOVX    A,@DPTR                 ;get ECR threshold values
         ANL     A,#F0H                  ;mask to save high nibble
         ORL     A,RO                    ;or high and low nibble
         MOV     RO,A                    ;save as new ECR count
         MOV     DPTR,#T1_OOF_ERRORS
         MOVX    A,@DPTR                 ;get OOF running count
         INC     A                       ;....and increment by 1
         MOVX    @DPTR,A                 ;put new count back
;
; Finally, write new value of ECR back into the T1 (DS2180) Transceiver.
;
ECS_WT:  MOV     A,RO                    ;transfer new count to ACC
         MOV     R1,#T1_ECR              ;load T1 ECR address
         LCALL   T1_RANDOM_WRITE         ;write one T1 register
INTO_R   RET                             ;return to main program
```

Dallas Semiconductor Security System Locks Up Software

Application Note-8

ELECTRONIC DESIGN EXCLUSIVE

Security is a fact of business life. Information and property must be protected from fraud, theft, and misappropriation. Personal computer software represents both these kinds of items, and yet the multibillion-dollar industry has virtually no protection.

Of the methods employed to protect software from illegal copying, the most popular ones use programming tricks. Unfortunately, those methods also stop the legitimate user from backing up valuable disks. To make matters worse, programs have been developed to defeat most software-based schemes for copy protection.

A better solution lies in the marriage of software and hardware. With such a merger in mind, security takes the form of a special key. The DS1204 system permits only legitimately purchased software to be run, and it does not unduly disturb the personal computer user or prevent him or her from making backups to hard disks (see *Electronic Design*, September 5, 1985, p. 219). A package about the size of a postage stamp, which contains an IC and a lithium energy source, stores identification and an unrevealable code word that protects a secure, nonvolatile read/write memory. Upon installation of the DS1250, a simple key ring that consists of a five-contact key receptacle connected through a cable to an intermediate socket, the key ring and key lock-out precoded software from all but rightful keyholders.

The byte wide key ring implementation begins with a system board that contains a 28-pin socket with or without a resident ROM. (In all personal computers, there is at least one ROM that is used for boot sequences, basic I/O system implementation, or some form of dedicated software monitoring.)

READY TO GO

With the key ring inserted in the ROM socket, the ROM inserted into the key ring, and the key inserted into the clip at the end of the cable, the system ROM functions normally. The address and data lines are transparently sent through the byte wide key ring socket and presented to the system ROM as usual. As a result, existing unprotected software will run on the system.

However, if certain address lines are driven with specific patterns, the software activates the key ring, which disconnects the ROM from the system board and ties the address and data lines to the key ring's own bus. At that point, communication to the system board ROM socket is transparently passed on to any device that is inserted into the key clip.

A MEMORY BARRIER

A partitioned memory in the key sets up a system of barriers, preventing unauthorized access to software. The first barrier is possession of the key, since the silicon chip inside the key is extremely difficult to copy. If a copy is nevertheless made, the code words and nonvolatile memory are lost during what may otherwise seem to be a successful process of reverse engineering.

The key stores 64 bits of user-definable identification code, and a 64-bit security match code that protects 128 bits of read/write nonvolatile memory. The 64-bit security code in the key, once programmed for one particular disk by the software vendor, cannot be read or derived by the user.

Another barrier can be thrown in the pirate's path: the key manufacturer, using a laser, can brand another 13 bits of key memory with a code unique to the software maker.

A final level of protection is afforded through intricate programming techniques. Because the electronic key functions as a read/write memory, it can "converse" with deeply embedded software locks and actually change its own password from use to use.

EASY TO USE

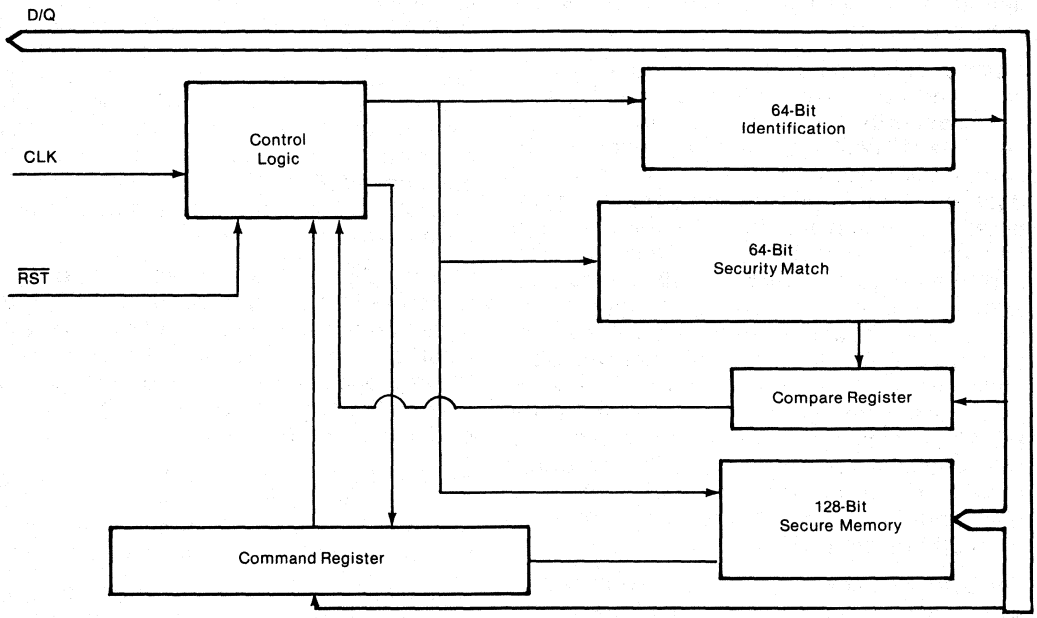
A low pin count and a guided entry to its socket make the device transportable and user insertable. A lithium battery supplies power for decades.

The electronic key has two modes of operation. In the normal mode, data transfer takes

place between the key ring and the key (Fig. 1). To initiate a data exchange, $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the command register from the computer. That 24-bit protocol stores an unalterable code that includes the 13 burned-in bits. If the key's command register proves to be loaded properly, communication continues (Fig. 2).

Following the 24-bit exchange, 64 read cycles examine the identification RAM in the key. The computer then writes 64 bits to the compare register, also on the key. If that block agrees with the security match RAM, permission is given to read or write the 128-bit nonvolatile memory. If a match is not found, access to additional information is denied. The 128-bit section can be changed indefinitely to meet the needs of a dynamic protection scheme.

Figure 1



NOTE:
In the normal mode, data from the computer is applied to the key through the key ring. That data is compared in the command and compare registers. Data from the key is then returned to the computer to complete the verification procedure.

Driving $\overline{\text{RESET}}$ high also initiates the program mode (Fig. 3). The computer software loads 24 bits into the command register on each low-to-high transition of the clock input. If the key's command register is not properly loaded, the remainder of the program cycle is ignored. However, if the command register is properly loaded, then the following 128 bits are written to the identification memory and the security match memory after the data in the 128-bit nonvolatile RAM has been erased by the key.

Dynamic interaction with the key can be maintained throughout program execution. The matching codes of the key and the program on disk are continually updated with a pseudorandom number—say, the check sum of the system address space at a given instant in time.

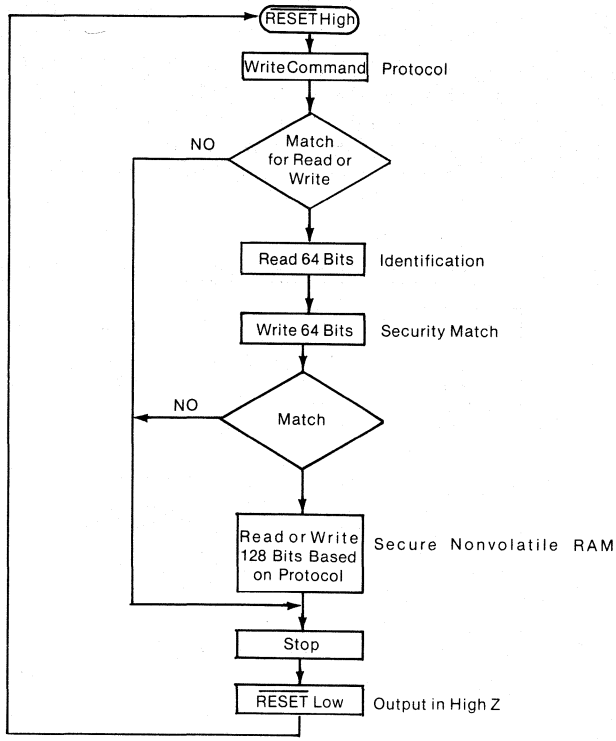
At various points in the program, the checksum value in the application program is matched with the value in the key. If they do not match, program execution is aborted. If they do, another check sum is written to the application program on the disk and to the key, and execution of the program continues.

Alternatively, program parameters or instructions themselves can be stored in the key's 128 bits of nonvolatile memory. Those code fragments are called up, or dynamically loaded, and initiate actions that are crucial to the proper functioning of the application program. If the key is improperly programmed or programmed with invalid information, those code sequences will cause the program to deliver unpredictable and incorrect results to the unauthorized user.

RUNNING RINGS AROUND THE DATA

The key ring adapts the electronic keys, with their low pin count, to JEDEC standard byte wide memory signals. Any 28-pin RAM, ROM

Figure 2



NOTE:
The key is matched against a particular program in a sequenced two-way transfer of data. Previously stored data supplied by the software enables each key to be tailored to a program.

or EPROM device can be removed and placed in the intermediary socket of the key ring. The combination can then be reinstalled in the original ROM location, leaving the system intact. Optional key rings are available for 16-pin dynamic RAM and 24-pin ROM sockets, and for the parallel printer port of IBM or IBM-compatible personal computers.

The intermediary socket contains a CMOS chip that redirects information flow from the byte wide memory to the inserted keys, according to special software-generated address sequences. Data transfer of 50 Kbits/s are possible with an assembly language software driver of less than 500 bytes.

The key ring protocol is derived from address inputs A_0, A_1 and A_2 (Fig. 4). Those addresses are latched on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}_{in}$ and $\overline{RAS}/\overline{OE}_{in}$. A_0 defines the data that is compared for recognition. A_1 activates the communication sequence, while A_2 clocks in information defined by A_0.

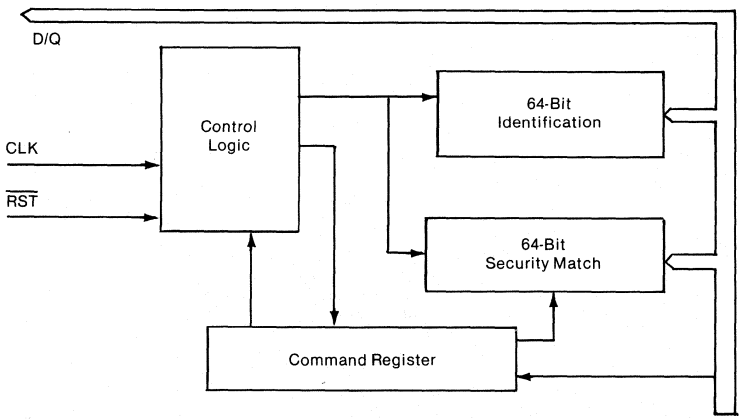
As noted, data transfer through the key ring occurs by first matching a 24-bit pattern from the software. That pattern is presented to a register on each rising edge of a strobe. Therefore, data is entered for comparison to the key ring protocol at the end of each memory cycle.

While keeping A_1 high, the proper information must be presented on A_0 to match the 24-bit pattern. Address input A_2 generates the shift signal that supplies data to the 24-bit register for comparison with the pattern that has been placed in the key by the manufacturer.

Information is loaded one bit at a time on the rising edge of the shift pulse, and each shift cycle must be generated from two memory cycles. The first memory cycle sends A_2 low, setting the shift clock low. The second memory cycle sends A_2 high, causing the transition necessary to shift a bit of data into the 24-bit register. A_0 is kept at the same level for both memory cycles. Address input A_3, which controls the direction of data going to and from the keys, is not used during pattern recognition in the key ring protocol.

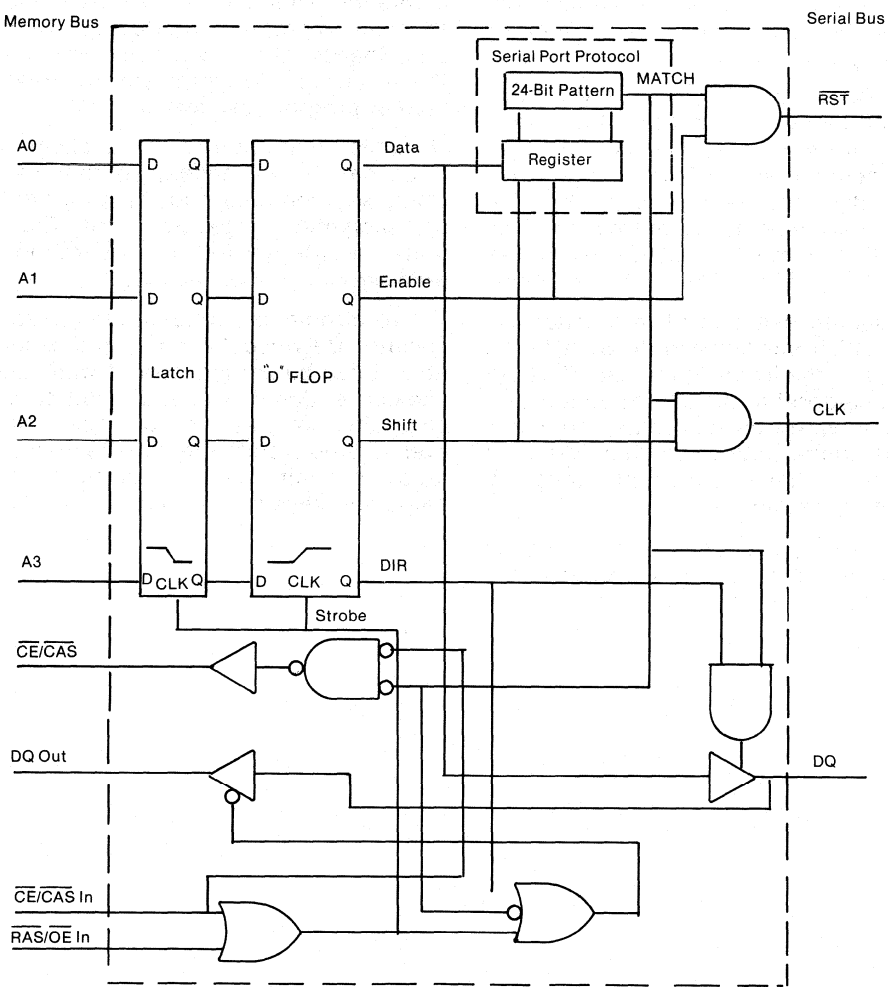
After the 24-bit pattern has been correctly entered, a match signal is generated and logically combined with the enable signal to generate $\overline{RESET}$ for the key. The match signal is also used to disable the original memory device (now plugged into the key ring) and to enable a gate allowing the key's

Figure 3



NOTE:
In the programming mode, after the first 24 bits are written, the key checks to see that they contain a valid programming code. If so, 128 bits are written to the identification and security match RAMs.

Figure 4



NOTE:
The key ring provides an active interface between the host computer and the key. Key data plus control pulses are provided by the address line.

Data I/O line to drive the computer memory bus. When $\overline{\text{RESET}}$ is driven high, devices attached to the key ring become active and subsequent shift signals derived from A_2 will be recognized as the key clock.

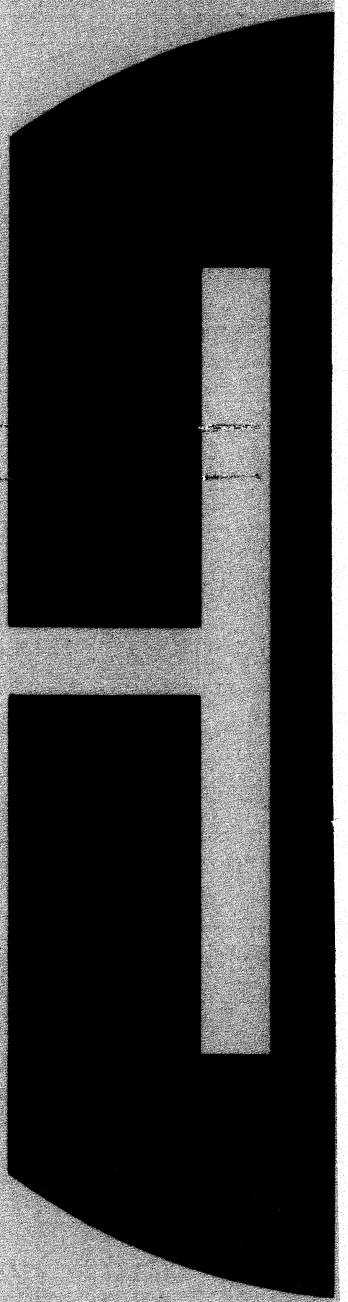
The data signal for the key on the A_0 line depends on the level of the direction signal on A_3. When A_3 is high, data as defined by A_0 will be sent out on the Data I/O line. When A_3 is low, devices attached to the key ring can drive the memory bus output line. The data direction bit must be set low to read key data.

A sophisticated example of interaction between the electronic key and the application software package involves the use of a data encryption algorithm. The application program is encrypted as distributed from the factory, using the Data Encryption Standard or the Rivest, Shamir, Adleman public key encryption algorithm.

The public key is contained on the program media and the private key goes into the electronic key's memory. A kernel, invoked when the application program is activated, decrypts the remainder of the binary version of the running program, producing a functional one. That program then communicates with the electronic key, providing a greater degree of program security.

Dynamic encryption of the application program can be expanded, so that the electronic key contents and the program image are encrypted on program exit. The result: both are different for each operation of the program.

The electronic key is not limited to software security. Because it is small and user-insertable, it can be carried, stored, and used just like conventional keys and credit cards. The electronic key has the added benefit, however, of a nonvolatile read/write memory and a data capacity that surpasses most credit cards and keys in use today.



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